Session 1A5
Microelectronic Packaging

A Hybrid Time-domain Method for Electromagnetic Problems in Microelectronic Packaging

T. Xiao, **M. Chai**, **and Q. H. Liu**
Duke University, USA

Computational electromagnetics for the design simulation of microelectronic packaging problems faces a great challenge because of the complex fine geometrical details in the chip level compounded with the large scale of the package. A time-domain approach such as the finite-difference time-domain method with a uniform grid requires a large number of discretization points to solve such mixed-scale problems. This issue is especially challenging for package-level problems.

In this work, we develop a hybrid time-domain technique that combines several methods for the efficient modeling of microelectronic packaging problems: (a) the enlarged cell technique (ECT) for the conformal FDTD method, (b) the alternating direction implicit conformal finite-difference time domain (ADI-CFDTD) method, and (c) the pseudospectral time-domain (PSTD) method. The ECT eliminates an important limitation, i.e., the reduction in the time step size, in the CFDTD method, and removes the staircasing error in the FDTD method for curved conductors. Similarly, the ADI-CFDTD method removes this staircasing error, and is especially useful for regions with electrically small features. The PSTD method, on the other hand, is efficient for large homogeneous regions. Therefore, combining all these methods in our hybrid time-domain technique is attractive as it makes use of their advantages while avoiding the disadvantages in each of these methods. The interface conditions between different regions of these methods are provided by the Riemann solver to ensure the stability. We will demonstrate the efficacy of this hybrid method by solving large-scale package level EMI/EMC problems.

Effects from the Thin Metallic Substrate Sandwiched in Planar Multilayer Microstrip Lines

L. Zhang and J. M. Song
Iowa State University, USA

Abstract—This paper studies the dispersion characteristics of open multilayer microstrip lines with a thin highly-conductive metallic substrate using the spectral domain approach. From the numerical results, it is found that, in both lossy (metal-insulator-silicon structure such as Si-SiO_2) and lossless configurations (thin metal between lossless dielectric microstrip line), at the low frequency range, this thin metallic substrate can excite slow waves. And accordingly the frequency dependent transmission-line characteristics of interconnects, such as propagation constant, attenuation and the characteristic impedance, can change remarkably with the existence of the thin metallic substrate.

1. Introduction

The lossy transmission line structures gain more attentions due to the fast development of the VLSI semiconductor circuits. In this case, multilevel interconnect networks are introduced into multilayer silicon structures to enable great efficiency of semiconductor integration. But this is also accompanied with many challenges to interconnect in circuit design. From the viewpoint of signal integrity, these complicated structures of interconnect network make the circuit much vulnerable to the substrate coupling of noise, power supply noise, ground bounce, crosstalk, ringing, antenna effects etc.

As one solution, very thin highly-conductive substrates are added into multilayer structures as ground to depress or shield away the harsh effects. Cregut et al., showed that, by certain metallic substrate configuration, the crosstalk can be reduced as well as the transient performance improved [1]. However, at some low RF and microwave frequencies, the skin depth may be much larger than the metal thickness of profile. The electromagnetic wave can penetrate the thin metallic substrate and reach further deeply into the layers underneath. In another words, the electromagnetic wave can "see through" and consequently interact with the multilayer configuration underneath. Considering this phenomenon, Song et al. found the frequency dependent characteristics or dispersion characteristics of interconnects, such as resistance, inductance, capacitance, and conductance (RLCG) per unit length, change remarkably with the existence of thin metallic substrate [2].

The previous work of planar multilayer microstrip line starts with the hypothesis of the perfect electric conductor (PEC) ground plane or impedance boundary condition (IBC), and considers the effects of the strip with finite conductivity or thickness. This paper focus on the effects of this thin but highly conductive substrate in the middle substrate. To adequately analyze this effect, the spectral domain approach (SDA) is used [3, 4]. The simplified model of an open microstrip line is proposed, and the corresponding 2-dimensional Green's functions of multilayer microstrip line are deduced. The method of moments is applied to solve the related eigenvalue problem numerically. Thus the dispersion performances of the propagation constant, attenuation and the impedance of open multilayer microstrip lines are simulated numerically. It also shows that the slow wave can be excited.

2. Modelling and Spectral Domain Approach

The open microstrip line with considered thin metallic substrate is shown in Figure 1. The substrates are assumed to be uniform and infinite in both the x and z directions. The signal strip as well as the lowest ground plane is taken as infinitesimally thin and PEC. After taking a spatial Fourier transformation in the x direction, the coupled integral equations on the surface of the strip line become the algebraic ones as following

$$\begin{bmatrix} \tilde{E}_x(\alpha, y_s) \\ \tilde{E}_z(\alpha, y_s) \end{bmatrix} = \begin{bmatrix} \tilde{Z}_{xx}(\alpha, y_s) & \tilde{Z}_{xz}(\alpha, y_s) \\ \tilde{Z}_{zx}(\alpha, y_s) & \tilde{Z}_{zz}(\alpha, y_s) \end{bmatrix} \begin{bmatrix} \tilde{J}_x \\ \tilde{J}_z \end{bmatrix} \tag{1}$$

where $\tilde{Z}_{xx}$, $\tilde{Z}_{xz}$, $\tilde{Z}_{zx}$ and $\tilde{Z}_{zz}$ are the dyadic Green's functions for microstrip geometry. α denotes the spectral domain variable in x direction. y_s stands for the interface where the signal strip located on. The immittance approach [3] decouples the field into two independent configurations as transverse electric (TE^y) and transverse magnetic (TM^y) modes. Using the transmission line modelling (TLM), the Green's functions are derived as parallel combination of the admittance seen above and below the interface y_s. Then the Galerkin's method

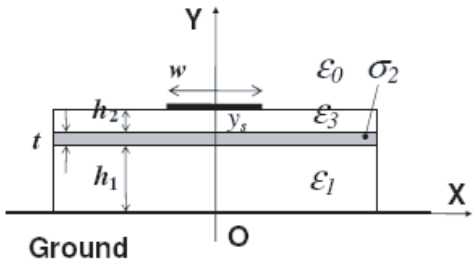


Figure 1: Configuration of 3-layer open microstrip line with very thin metallic substrate with thickness t (grey).

is used to solve the equation (1) for the propagation constant. The current density $\tilde{J}_x$ and $\tilde{J}_z$ are separately expanded into a series of basis functions as

$$\tilde{J}_x = \sum_{m=1}^{M} a_m \tilde{J}_{xm}, \quad \tilde{J}_z = \sum_{n=1}^{N} b_n \tilde{J}_{zn}, \tag{2}$$

where the a_m and b_n are the coefficients of current basis function. After substituting the current expansions (2) into (1) and doing the scalar product on both sides, based on the Parseval theorem, the integral equation is discretized into a homogeneous system with $M + N$ linear equations. Consequently the value of propagation constant is directly correspondent to the eigenvalue of the system which makes the determinant of the following equation equal to zero.

$$\begin{aligned} \sum_{m=1}^{M} a_m K_{i,m}^{xx} + \sum_{n=1}^{N} b_n K_{i,n}^{xz} = 0 \quad (i = 1, \ldots, M) \\ \sum_{m=1}^{M} a_m K_{j,m}^{zx} + \sum_{n=1}^{N} b_n K_{j,n}^{zz} = 0 \quad (j = 1, \ldots, N) \end{aligned} \tag{3}$$

The real part of the complex wave number is related directly with the propagation wavelength and phase velocity while the imaginary part is the attenuation per unit length along the z direction.

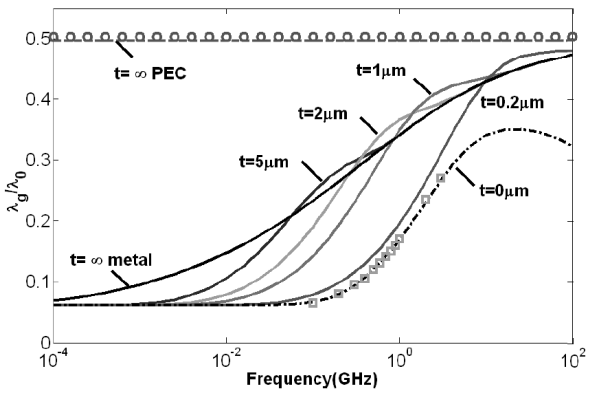
3. Dispersion Characteristics

In this section, the influences of this very thin metallic substrate on the performance of microstrip are simulated. One thin metallic substrate is inserted into a metal-insulator-semiconductor (MIS) structure and a lossless microstrip line, which results in two multilayer cases respectively: the metal-insulator-metal-semiconductor (MIMS) and metal-insulator-metal-insulator (MIMI) to be studied in the following.

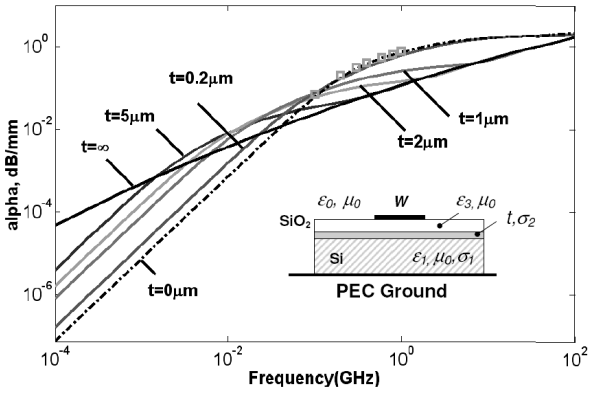
3.1. Very Thin Metallic Substrate in Lossy System

Here one modified case of MIS structure is considered with a thin metallic substrate inserted between the dielectric SiO_2 and lossy Si as shown in Figure 2(b). The ϵ_r of the silicon dioxide is 4 and its thickness is $1\,\mu$m. The width of strip is $160\,\mu$m. The thickness of the silicon layer is $250\,\mu$m with $\epsilon_r = 12$ and conductivity $\delta = 5\,$S/m. Figure 2 shows the frequency dependence of the attenuation constant and the normalized guiding wavelength, which is equivalent to the phase velocity normalized by the speed of the light in free space. When the t equals to zero, this modified structure is degraded into the typical metal-insulator-silicon structure previously studied by the Hasegawa et al. [5]. Our results agree well with the one calculated by Cano, Medina and Horno shown as rectangular dots in Figure 2. The further validation can be found in [7].

In Figure 2(a), as the frequency decreases, the normalized guiding wavelength converges to about 0.06. So the wave propagates on the microstrip lines much slower than in free space, which is known as the slow wave effect. In addition, several "limit" curves are marked. When the thickness of the middle metallic substrate grows to infinity, the effect of the silicon substrate and PEC ground underneath become negligible. Another curve is obtained by treating the middle metal as PEC to make the transmission system become lossless. This curve fits well with the result of Pramanick's and Bhartia's formula [8] shown as circle dots. With increasing the frequency, each curve with different thickness converges consequently to the critical curve representing the infinite metal thickness. This attributes to the fact that the skin depth decreases as the frequency increases. Physically it means the electromagnetic field experiences more attenuation when penetrating the same conductive metallic substrate. Thus at some points, the whole substrate can become opaque and block the field from reaching the lower substrate. At the high frequency, the thin metallic substrate will work as infinite thick metal ground, when the metal thickness equals to 2 to 3 times of the skin depth. For example, at 1 GHz, the skin depth of

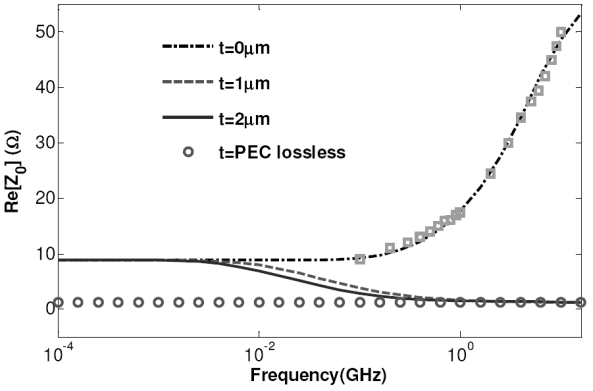


(a) Normalized wavelength

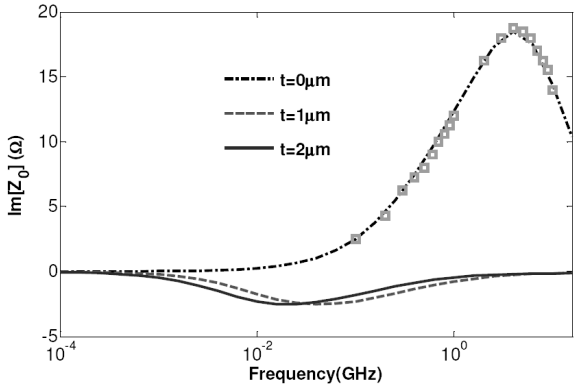


(b) Attenuation constant

Figure 2: Dispersion performance of a 3-layer MIMS open microstrip under different thicknesses t. (lower silicon thickness: 250 μm; ε_r: 12; σ: 5 S/m; thin metal σ: $5.8(10^7)$ S/m; upper silicon-dioxide: 1 μm, ε_r: 4; w: 160 μm; circle dots: Pramanick and Bhartia's results [8] for lossless microstrip lines; rectangular dots: Cano, Medina and Horno's results [6] for MIS structure).



(a) Real part



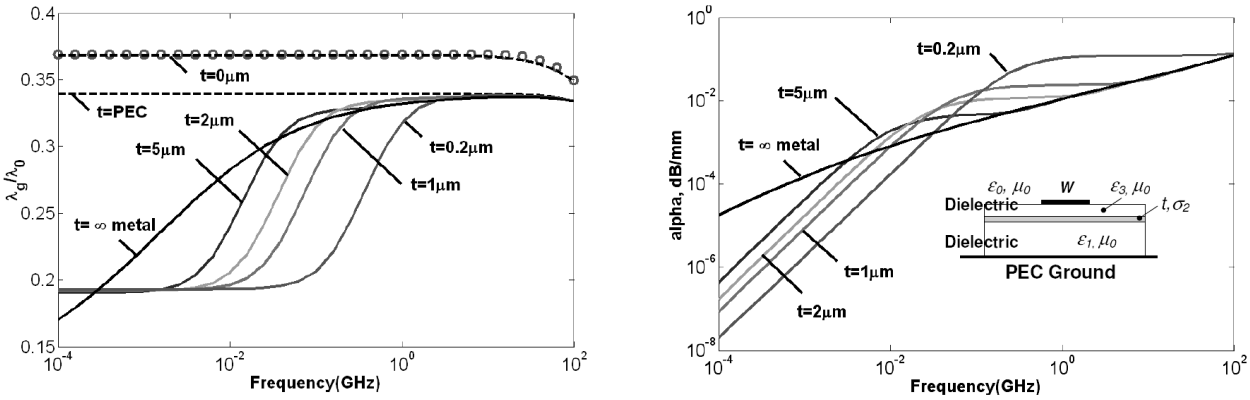
(b) Imaginary part

Figure 3: Frequency behavior of the (a) real and (b) imaginary parts of the characteristic impedance for the MIMS structure shown in Figure 2 (using $Z_0 = V/I$ definition, rectangular dots: Cano, Medina and Horno's results [6] for MIS structure).

copper is about 2 μm. The curve with thickness of 2 μm converges at around 4 GHz, almost 2 times thicker than the skin depth at 4 GHz. Similarly for 1 μm curve, the convergence point is about 25 GHz with skin depth 0.4 μm. In most of the frequency range shown, the normalized guiding wavelength decreases as the frequency decreases. When the skin depth is about 10 times more than the metal thickness, the wave becomes a slow wave.

Figure 2(b) also shows the behavior of the attenuation. The attenuation constants under different thickness of thin ground substrate approach consequently to the critical curve of infinite thickness. At the high frequency range, the attenuation is proportional to square root of the frequency. This is because the electric current flows through a region proportional the skin depth that is proportional to the inverse square root of the frequency. On the contrary, at the low frequency region, it is observed that the slopes of the curves are proportional to the square of the frequency, which is due to the ohmic loss of the electric current flowing in the metallic ground and substrate. In addition it is observed that the curves for finite thickness converge to the infinite thick metallic substrate when the thickness is equal to the skin depth. For example, the curve of 2 μm converges to the infinite thick at about 1 GHz. It shows that the concept of skin depth has more direct connection with the attenuation constant other than the phase velocity in Figure 2(a).

Figure 3 shows the relation of characteristic impedance versus frequency computed by using the definition of voltage-current. The voltage is defined as the path integral of the electrical field E_y on the y axis from the



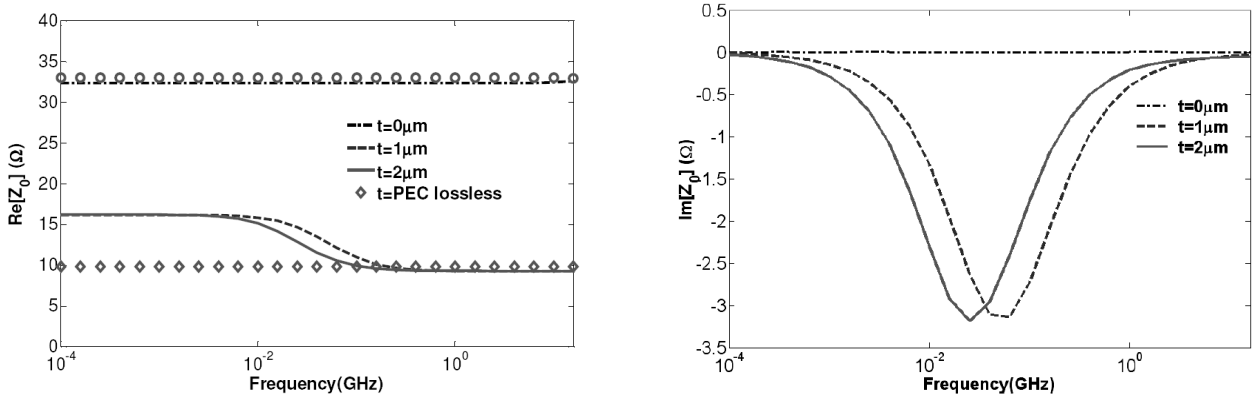
(a) Normalized wavelength (b) Attenuation constant

Figure 4: Dispersion performance of a 3-layer MIMI open microstrip under different thicknesses t of thin metallic substrate. (lower dielectric substrate: 80 μm; ε_r: 10.2; thin metal σ: $5.8(10^7)$ S/m; upper dielectric substrate: 20 μm, ε_r: 10.2; w: 200 μmm; circle dots: Pramanick et al. results [8] for lossless microstrip lines).

strip center to the ground plane and the current is the longitudinal current flowing through cross section of the strip. When the thickness t becomes zero, our result is validated by the result from Cano et al., [6] again. The figures show that when the thickness of the thin metallic substrate becomes larger, the characteristic impedance decreases. This behavior is very like the one when directly increasing the conductivity of silicon layer in MIS structure. The thicker this metallic substrate is, the more current flows through its cross section. Or equivalently, the impedance of this thin metal becomes smaller. When t becomes PEC, the impedance become pure resistance with the smallest value as shown (circle dots) in Figure 3(a).

3.2. Very Thin Metallic Substrate in Lossless System

As demonstrated before, the slow-wave is a comprehensive effect due to the influence coming from the lower lossy silicon substrate and this thin metal. To identify the influence of this thin metallic substrate only, a thin metal layer is inserted into a lossless microstrip line as shown in Figure 4(b). The lossless dielectric material ($\varepsilon_r = 10.2$) is divided into two parts as 20 μm and 80 μm. The width of the metal strip line is 200 μm. The corresponding dispersion characteristics are calculated and shown in the Figure 4(a) and 4(b). The similar patterns reoccur and accord with the previous figures and discussions. This also illustrates that the thin metal layer with finite conductivity in a lossless substrate can introduce the slow wave phenomenon at the low frequency range.



(a) Real part (b) Imaginary part

Figure 5: Frequency behavior of the (a) real and (b) imaginary parts of the characteristic impedance for the MIMI structure in Figure 4 (using $Z_0 = V/I$ definition, circle and diamond dots: Pramanick and Bhartia's results [8] for lossless microstrip lines with 100 μm and 20 μm dielectric substrates repectively).

In addition the remarkable difference between the PEC and real metal shows that the slow wave exists even

when the thickness is only small fraction of the skin depth. This is a phenomenon that the PEC cannot describe appropriately. It is concluded that this thin metallic substrate has great impact on the dispersion characteristics of microstrip lines.

In Figure 5, the real and imaginary parts of the impedance are also plotted. when t equals to zero, our result agrees with the Pramanick's. The imaginary parts of the impedance is relatively small compared with the real parts. At the same time, when the metallic substrate becomes thicker, the impedance converges to the PEC (diamond dots in the figure) faster at the higher frequency range. This is because the reduction of the skin depth with increasing frequencies makes the thin metallic substrate more likely act as the good conductor with infinity thickness.

4. Conclusion

The effects of a thin metal ground with finite conductivity on the dispersion characteristics of loss and lossless multilayer microstrip line have been examined using the rigorous spectral domain approach. The numerical results show that electromagnetic field can penetrate the metal layer and interact with layers underneath. It is found that the thin metallic substrate in both lossy and lossless cases has a great impact on the dispersion characteristics, such the propagation constant, attenuation constant and characteristic impedance of multilayer microstrip lines even the thickness is much less than the skin depth. If considering the signal phase constant or velocity, the thin metallic substrate with thickness greater than 2 to 3 times of the skin depth can be regarded as infinite thick. At the same time, if merely the attenuation considered, the thin metal with only one skin-depth thickness is enough to make the ground like infinite thick. The results show that, at the low frequency range, the thin metallic substrate can excite a slow wave in both lossy and lossless multilayer microstrip lines.

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Modeling of Randomly Rough Surface Effects on Absorptions by Conductors at Microwave Frequencies

X. Gu and L. Tsang
University of Washington, USA

H. Braunisch
Intel Corporation, Components Research, USA

Methods for modeling the impact of randomly rough conductor surface on the power absorption by conductors of high-speed interconnects are presented. The roughness of the interface, especially in microelectronic packaging based on organic materials, is often used to facilitate the adherence of the copper structures to the dielectric layers. Since the speed of interconnects is rapidly increasing to the multi-GHz region, the propagation and radiation at the shorter wavelength can cause the roughness of the surface to have significant effects on signal integrity. Existing commercial software tools do not allow users to model the surface roughness of the substrates accurately. There only exist simple empirical models with limited or unknown validity.

We model the effects of a random rough surface on the absorption by a metallic surface at microwave frequencies using 2-D and 3-D small perturbation methods. The results depend on the characteristics of rough surfaces: the RMS height, correlation length and correlation function. We further show the similarity with and differences from Morgan's classical result. The power absorption by a metallic surface is quantified through the development of the solution of electromagnetic fields on the rough dielectric-metal interface. The analysis leads to the extraction of frequency-dependent power attenuation for each given metal roughness profile.

We demonstrate the method for random Gaussian and exponential rough surfaces. We also extract the rough surface profiles from real measured surface data on PCBs and packages. Results are illustrated for the frequencies of interest that extend up to 50 GHz. Statistical results are further obtained from Monte-Carlo simulations. The roughness profiles are up to 4 microns in RMS height with correlation lengths 0.3 to 3 times the RMS heights.

Krylov Model Order Reduction of Finite Element Models of Packaging Structures with Embedded Frequency-dependent Multiports

H. Wu and A. C. Cangellaris
University of Illinois at Urbana-Champaign, USA

In an effort to tackle the complexity of the electromagnetic analysis of the signal and power distribution networks (referred to, in the following, as SDN and PDN, respectively) in state-of-the-art integrated electronic systems, their decomposition into several parts and the development of hierarchical models for some of the resulting portions is often utilized. The term "hierarchical" is used here to define a model development process where the electromagnetic properties of different portions of the structure under modeling are described in terms of models of different degrees of complexity and, hence, accuracy, the choice of which is dictated by the specific attributes of the structure and the modeling objectives. A most representative example of a structure for which such hierarchical analysis can be applied is the electromagnetic quantification through modeling of noise generation and coupling in multi-layered substrate with multiple power and ground planes and multiple signal layers sandwiched between the planes. Assuming that multi-conductor transmission line (MTL) models can be used for the coupled interconnects in the nets, the complexity of the finite element mesh for the multi-layered substrate is simplified significantly. An integrated model for the combined SDN and PDN system, which is needed for the accurate quantification of switching noise generation and coupling is then obtained by embedding the MTL models in the finite element model, through the proper interfacing of the two models at the signal vias. Considering the fact that different types of models can be used for the coupled interconnects (ranging from lumped RLCG models for short sections, to more accurate transmission line theory-based models, or even comprehensive electromagnetic models extracted either through a full-wave solver), the hierarchical nature of the resulting model is evident.

This paper presents a methodology for the direct generation of reduced-order macromodels of the hybrid models obtained from the application of the aforementioned hierarchical modeling process. More specifically, we are concerned with finite element-based models that include frequency- dependent macromodels for portions of the SDN and/or PDN, described in terms of a multiport transfer function matrix with its elements cast in terms of rational functions of the complex frequency $s = j\omega$. The proposed methodology utilizes Krylov subspace-based methods for the direct generation of compact (low-order) macromodels of the overall structure. Like in the application of Krylov subspace methods for the direct model order reduction of finite element models of packaging structures including lumped elements [1], the resulting methodology allows for the construction of the overall multiport macromodel over a broad frequency interval, at essentially the cost of a single frequency point solution of the finite element system.

The proposed methodology will be presented and its validity and efficiency will be demonstrated through its application to typical SDN and PDN structures. The paper will conclude with a discussion of some issues pertinent to the passivity of the generated reduced-order macromodel.

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Enabling Accelerated Boundary-element Design Tools for Packaging and Interconnects

S. Chakraborty and V. Jandhyala
University of Washington, USA

For today's high-speed, high-density electrical packaging, while analysis tools based on boundary element methods are particularly efficient due to the development of fast algorithms that solve these matrix equations in near linear time, the need for design tools has not been met. For boundary element methods, such a tool would necessitate the ability of incremental solution, wherein small changes in designs would not require a complete simulation pass. The development of such a design tool is rendered more challenging because boundary element methods, solved by method of moments techniques, lead to full matrices. Changing the location or design of a component would alter entire rows and columns of these matrices, and therefore increase even the setup cost linearly.

A novel approach to localize the effects of incremental design of spatially separated components within the method of moments is presented. The technique proceeds by isolating the component under design in a closed mathematical surface. This surface bifurcates the overall simulation problem: the interior problem includes the interaction of the component and its surface, and the exterior problem is related to the surface and the remainder of the global problem. The overall gain of this method is that the setup cost is only related to the local problem of the component, the surface, and the interaction between these two. Moreover, for direct solvers, a Schur-complement based scheme can also accelerate subsequent solves, by presenting the remainder of the matrix in a factorized form as a numerical Green's function for the localized problem.

Noise Source Characterization on the PDN for EMI

M. Lai[1], **V. Ricchiuti**[2], **A. Orlandi**[3], **B. Archambeault**[4], **G. Antonini**[3]
D. J. Pommerenke[1], **and J. L. Drewniak**[1]

[1]University of Missouri Rolla, USA
[2]Siemens C.N.X., Italy
[3]University of L'Aquila, Italy
[4]IBM, USA

Noise resulting from IC activity is easily distributed throughout an electronic design as a consequence of a low-impedance power distribution network in a multi-layer printed circuit board. Both EMI and SI problems can result as a consequence. The passive portions of the PDN are being successfully modeled with full-wave formulations, as well as circuit extraction approaches, which provide design insight and methodologies for the PDN. However, in order to determine specific total capacitance needed, as well as quantify the voltage on the PDN, a suitable noise source model is needed for the ICs. This work details a frequency-domain approach for extracting current noise source models from swept-frequency methods.

The core and I/O activities in a common IC have different contributions to the global noise level in the full system. In order to better understand and quantify the specific weight of each, a methodology for estimating these two distinct but simultaneous noise sources is being developed. The estimation of the noise current by means of S-parameters and power spectra measurements is proposed here for a 208 pin, 155.52 MHz clock FPGA characterized by two voltage logic levels, 1.8 V for the core and 3.3 V for the I/O. From the measurement of the power spectra at the two logic levels in a position that can be considered coincident with the FPGA itself and from 2-port S-parameters measurement, it is possible to model the noise currents sources associated with the core and I/O respectively. The method is validated by estimating the same noise current sources also from a remote location from the FPGA itself, and it is done by adequately taking into account the effect of the transfer impedance between the ports and the FPGA. The effect of the SMA connectors used to perform the measurement is removed by means of a de-embedding procedure. The noise current sources are fully characterized in terms of magnitude and phase by means of a Hilbert transform procedure using the measured power spectra. In order to take in account only the effect of the activity of the FPGA, the power spectra are filtered from the effect of the external clock. The obtained noise current sources can also be characterized in terms of different load conditions by changing the number of I/O outputs simultaneously switching, allowing the estimation of an upper and lower limit for the sources.

Fast Method for Analysis of Electromagnetic Bandgap Structures Used in Power Delivery Networks

A. Tavallaee and R. Abhari
McGill University, Canada

Electromagnetic Bandgap (EBG) structures are increasingly used in high-speed digital and mixed-signal electronic circuits as the efficient means of power/ground noise suppression and port isolation. In order to provide these functions, the EBG structure is incorporated in the power delivery network (PDN) of an electronic circuit. In a conventional method of system implementation, this modified PDN is distributed within the layers of a printed circuit board, whereas in modern microelectronic chip design and system packaging, it can be embedded in the substrate. In all these scenarios, design engineers need to employ fast and accurate methods to account for the added frequency-selective features of the modified PDN in circuit simulations.

Floquet-Bloch theorem has been used for decades to obtain the dispersion equations of periodic structures and thereby to predict the passband/stopband frequencies. Recently, this analysis technique has been adapted to two-dimensional (2-D) transmission-linebased geometries and applied to a number of metamaterials and metallo-dielectric EBG structures to examine their overall modal characteristics. The method can rapidly predict the frequency band diagram. However, it does not include computing complex propagation constants.

In this work, a similar approach is adopted to characterize the PDNs containing EBG structures, as they can be efficiently modeled by 2-D transmission line circuits. Moreover, a general formulation is developed to account for the losses introduced in the network due to imperfect conductors, lossy dielectrics and lumped passive elements representing the series/parallel periodic loadings. The overall incurred loss in signal transmission through such networks is investigated by obtaining the frequency response, H(f). The method benefits from the fact that it is derived from analytical solutions, thus resulting in rapid production of band diagrams with accuracy comparable to fullwave simulators. Furthermore, it has the advantage that frequency is specified as an input parameter and the dispersion equation is solved for the complex propagation constant. Simulation results for a few EBG structures, such as the mushroom-type proposed by Sievenpiper, will be shown to demonstrate the efficiency and capability of the method.

Extraction of Chip Power Delivery Current and Activity Variations

I. Kantorovich, V. Drabkin, C. Houghton, and J. St. Laurent
Intel Corporation, USA

Abstract—It is extremely difficult to directly measure power delivery current on chip under operating conditions. We discuss an approach of extracting PDS current through measurement of impedance of power delivery system and voltage. Because impedance extraction, in turn, requires knowledge of power delivery current, we use a controlled process for which power delivery current can be predicted. The paper provides a method of current extraction for impedance measurement.

1. Introduction

Current on power delivery system (PDS) of a chip and activity variation are major indicators of chip and package performance. Knowledge of PDS current is also important to assess worst case power delivery noise [1]. Current on a functioning die is generated by chip operation. Therefore it cannot be measured directly. The only exception is the case when chip activity is unchanged (for example, when the only process on chip is clock operation). In this case PDS current averaged over clk period is DC current which can be measured directly in any accessible location of power delivery loop far from chip. Because in general on-chip current is AC we need to look for indirect methods of current extraction. Because measurement of PDS voltage is easy to perform on a functioning chip, PDS current can be extracted from measured PDS voltage if PDS impedance of a chip is known [2]. There are two major obstacles preventing from measurement of PDS impedance on a functioning chip. First, because chip and package are not separated, a longer interconnect is required to allow connection with the probe. On-die PDS impedance is very low, in milliohm or sub-milliohm range, which is thousands time less than impedance of connecting wires. The second obstacle is that to extract impedance one needs to know both PDS voltage Vcc and current Icc, so we return to the problem of current extractions. In conventional methods involving VNA [3], current is injected into the system and can be measured directly. Although an attempt to extract PDS current on operating chip using PDS impedance stumbles, looping back to the problem of measurement of PDS current, it has an advantage: Instead of extracting PDS current for an arbitrary unpredictable computer process we can now focus on a particular controlled process of our choice because impedance of PDS does not depend on variations of chip activity.

The paper discusses an approach of extracting PDS current through measurement of PDS impedance and voltage. For impedance measurement we consider a controlled process for which PDS current can be predicted. The paper provides a method of PDS current extraction for impedance measurement and considers a methodology of extraction of PDS current and switching activity variations for any computer process.

2. Choice of Controlled Computer Process for Impedance Measurement

The controlled computer process must enable one to measure a magnitude of current, and since only direct on-die current can be measured the computer process has to contain long intervals with unchanged chip's activity. The computer process should also be simple because to extract impedance and current one needs to use Fourier transform and solve de-convolution problem which is sensitive to noise. Therefore the computer activity profile must be as simple as possible to avoid impedance to be dumped by noise. In [4–7] we suggested to use a computer process in which chip activity changes step-wise. The step-wise computer process is a good candidate to meet the above requirements. This process has a wider bandwidth than any continuous process. Several methods of generation of step-wise computer activity have been presented. For EV7 microprocessor measurements we used a specially designed computer code [4]. Advantage of this method is that it does not require any special hardware arrangements. We also used a method in which step-wise activity was generated by toggling clock frequency between two levels [5, 6]. In this method the profile of chip activity is far less noisy than the computer code method. A particular case of clock toggling is switching clock on and off [7, 8].

3. Extraction of PDS Current for Step-wise Computer Process

The rise/fall time limits the bandwidth of PDS current and impedance measurement. For activity step generated by toggling clock frequency the transition time is about one clock period. For step-wise process

we need to make an assumption about current behavior in the vicinity of the transition period. In [4–6] it was assumed that current is unchanged beyond transition and changes linearly within the transition interval (trapezoidal current). This assumption was adopted in other applications of this approach. [7, 8]. However, more detailed consideration of the current behavior shows that the mean PDS current (averaged over the clock period) is not trapezoidal. This can be derived from the correlation between the mean PDS current Icc and mean voltage on PDS Vcc of a chip:

$$Icc = C * F_{cl} * Vcc, \tag{1}$$

where F_{cl} is the clock frequency and C is the effective "switched" capacitance, which depends on the number of switching gates at a given state. According to Eq. (1), PDS current is not trapezoidal because voltage profile is not trapezoidal. From measurements it is known that voltage response to step-wise changing activity (step response) has a rippled profile after transition, exhibiting one or more droops. This means that, PDS current may not contain long unchanged intervals far from transitions, which are needed to provide us with reference points for current measurement. Therefore even for a simple, step-wise, change of chip activity PDS current has a complicated profile and there is no sections on current profile for which current can be measured directly. To resolve the problem, note that according to Eq. (1) chip can be formally characterized by an equivalent conductance G:

$$G = C * F_{cl}. \tag{2}$$

Because effective capacitance and/or clock frequency change when computer activity changes, for a computer process where chip activity toggles between high and low levels, the equivalent conductance will also toggle. We prefer to use conductance instead of resistance, because the transition time for conductance, unlike for resistance, properly represents the bandwidth of the process. We will use a representation of a chip through variable equivalent conductance to extract PDS current for the step-wise process. Figure 1 shows a simplified equivalent circuit for the power delivery loop.

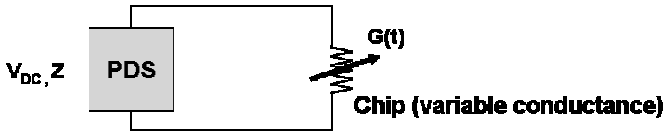


Figure 1: Simplified equivalent circuit of power delivery system.

The right hand side shows a chip represented by variable equivalent conductance. On the left hand side is a PDS block, which includes power delivery network on PCB, package and die. It also includes a DC voltage source. For the right-hand side, we can represent current as

$$Icc = G * Vcc \tag{3}$$

which is Ohm's law in time domain. This equation allows one to determine PDS current for a step wise process if variable conductance is known. Fourier component of PDS impedance Z can be determined from the convolution equation valid for PDS block in Figure 1. It is presented in the form of Ohm's law in frequency domain:

$$Z = -Vcc(f)/Icc(f), \tag{4}$$

where f is noise frequency. Eq. (4) is not defined at zero frequency. Note that we independently use Ohm's law twice to determine both PDS current and impedance. In this solution the problem of extraction PDS current is reduced to the problem of extraction variable equivalent conductance of the chip for a step-wise computer process. Because equivalent conductance changes step-wise, we need to know its high and low levels. We measure them separately in two independent computer runs, in which the only process running on-chip is a process with unchanging activity on either high or low level which will be used later on in activity toggling. In each run we simultaneously measure the mean voltage between power and ground on chip and the mean current. We cannot measure current on-chip, so we measure it far from chip, on voltage regulator, because current is unchanged. Each conductance level is determined as a ratio of measured current and voltage.

It is important to accurately measure Vcc profile to avoid noise in impedance profile, because current for any computer process is determined using division by impedance. Most of the noise is a random noise which can be excluded by averaging over many Vcc waveforms. Regular noise can be identified by changing clock

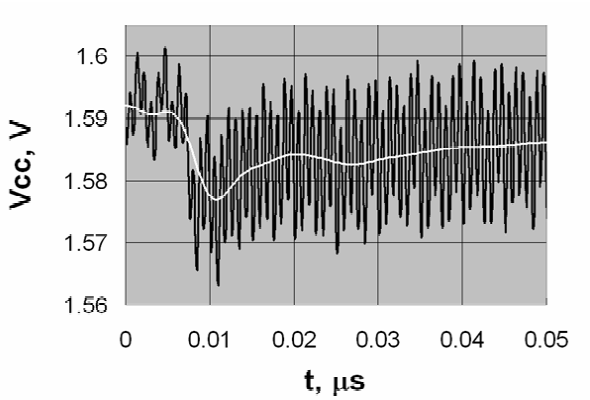


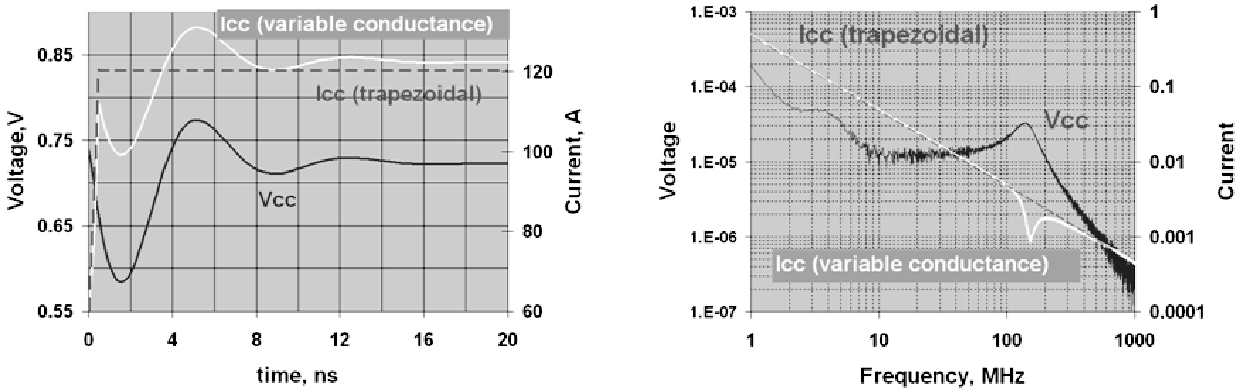
Figure 2: Typical measured raw Vcc (black) and Vcc after noise is filtered out (white).

frequency or measurement setup [6]. Figure 2 shows a typical measured raw Vcc (black trace) and Vcc after noise is filtered out (white trace).

In the methodology we have just discussed we measure directly only PDS voltage on-die and current on voltage regulator. With these measurements no calibration and compensation of parasitics is required which is a nightmare for traditional methods of low impedance measurements using VNA or impedance analyzers. Note also that by solving the problem of Icc extraction, we actually eliminated the problem of very long interconnect in measurement of very low impedance.

4. Comparison of Different Methods of Icc Extraction for Step-wise Process

Consider differences between impedance determined through variable conductance representation of a chip, and assuming trapezoidal current. We do not expect difference in impedance resonance frequencies because in variable conductance case current ripples follow Vcc ripples, so resonance frequency is the same as for Vcc resonances for both assumptions. However, resonance peaks may be different, because Icc varying in accord with voltage variations can make impedance resonances more pronounced than in the case of trapezoidal current. Figure 3(a) shows voltage and current waveforms in time domain for measurement simulation made for a Spice model of a future generation chip. One can see that Vcc has an overshoot, and it rapidly returns to its value before transition. This system has a high Q-factor. Figure 3(b) shows voltage and current in frequency domain. We can see that both voltage and current for "variable conductance" case have pronounced resonances. The trapezoidal current does not have resonances.



(a) (b)

Figure 3: PDS current and voltage for measurement simulation in time (a) and frequency (b) domains.

Figure 4 shows impedance of this chip for the two cases. One can see that assuming trapezoidal current on-chip (white trace) we get to a significant, 3-fold, underestimation of the resonance impedance.

Consider measurement results for EV7 microprocessor. This system has a 3-fold higher decoupling capaci-

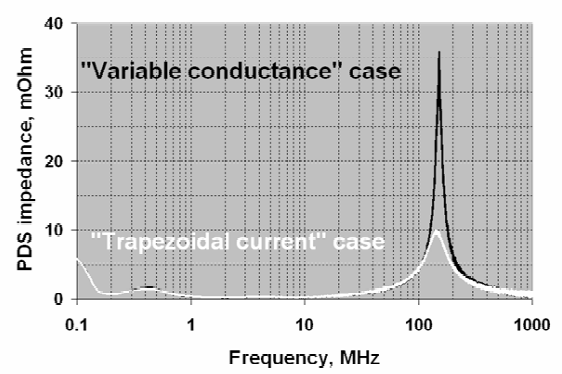
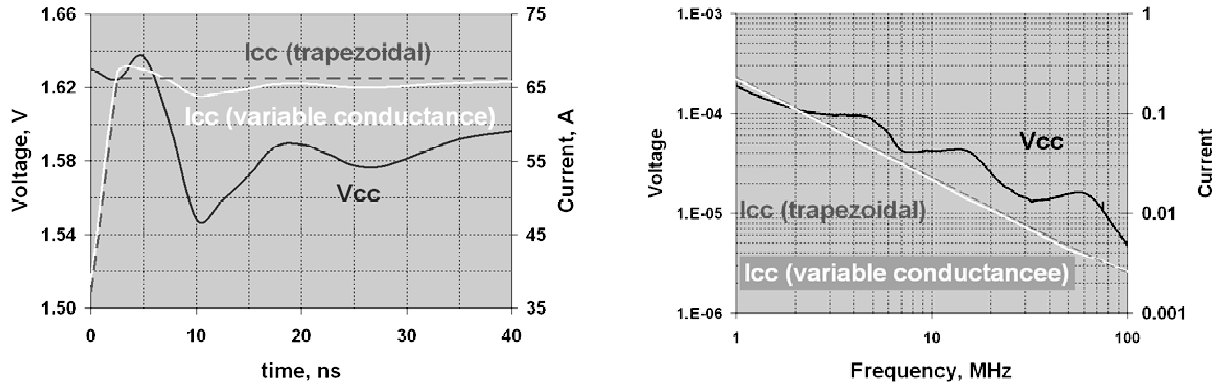


Figure 4: PDS impedance for measurement simulation.

tance and an order of magnitude higher resistance in the decoupling loop then in the previous case. Figure 5(a) shows that Vcc after the first droop restores slowly so that the noise at maximum is still half of the noise at the first droop minimum. The Q-factor for EV7 chip is lower than in the previous example. Figure 6 shows PDS impedance of the EV7 chip, extracted using the two assumptions on Icc. There is no significant difference between the results obtained using both methods. Figure 5(b) provides an explanation. It shows Fourier components of measured Vcc and the two currents. The voltage resonance at 60 MHz is shallow, so that the respective current resonance for "variable conductance" case is hardly noticeable on the steeply declined current profile. Figure 7 shows the relative difference between values of impedance determined by the two methods plotted versus Q-factor. The difference goes up linearly with the increase in Q-factor.



(a) (b)

Figure 5: PDS current and voltage for EV7 chip in time (a) and frequency (b) domains.

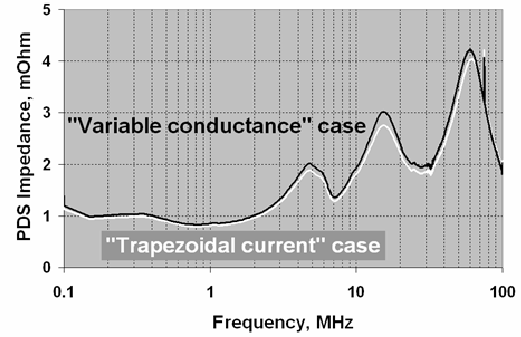


Figure 6: PDS impedance for EV7 chip.

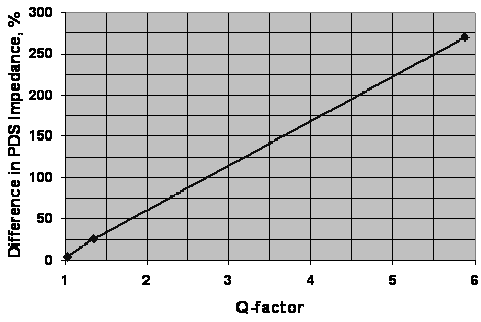


Figure 7: Relative difference in PDS impedance.

5. Extraction of PDS Current for any Computer Process

Once PDS impedance on chip is known one can extract PDS current for any computer process, not only step-wise process, by using a de-convolution procedure. Maximum ΔIcc can be obtained running extreme processes with maximum activity changes (power viruses). To extract the current signature we measure PDS voltage, and apply FFT to convert Vcc to frequency domain. Dividing voltage by known impedance we can obtain PDS current in frequency domain. Then we apply inverse Fourier transform in order to convert PDS current from frequency to time domain. Since PDS impedance is not defined at zero frequency, the de-convolved PDS current is determined up to an additive constant and a reference current is required to determine Icc. The way to obtain the reference current is to measure Icc at voltage regulator simultaneously with measurement of Vcc on-die. This current is averaged over time and is used as a reference for the averaged de-convolved PDS current. Figure 8 shows a fragment of measured Vcc on EV7 chip running the power virus SWIM, and Figure 9 shows the de-convolved PDS current on-chip.

6. Extraction of Activity Variations

We used a term "chip activity" to qualitatively characterize a computer process. Equivalent conductance can serve as a quantification of the chip's activity. It best represents the chip activity because supply current is consumed through switching of on-chip capacitive loads. Changes in activity result from changes in the magnitude of the capacitive loads or from changes in the frequency at which the capacitive loads are switched. Because equivalent conductance variation depends on the same changes, the variance in switched activity is equivalent to a variance in chip equivalent conductance. Actually, chip's activity rather than chip's PDS current can be considered as a stimulus producing PDS noise. The chip's current is less appropriate because it is affected by the Vcc. Therefore, for PDS noise characterization we need to know ΔG rather than ΔIcc. We can determine variations of the chip's activity or equivalent conductance dividing measured PDS current by voltage in time domain. Equivalent conductance variation for EV7 chip is shown in Figure 10. From Figure 10 one can extract maximum ΔG, knowledge of which is necessary to obtain the absolute maximum PDS noise for a chip.

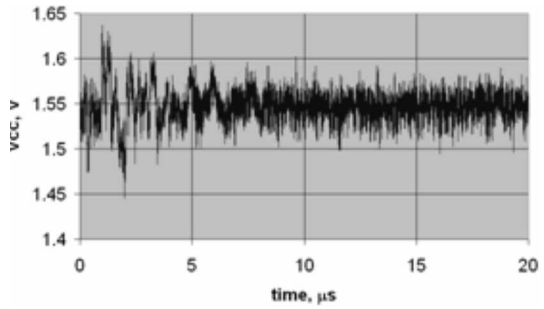


Figure 8: Vcc on EV7 chip running power virus SWIM.

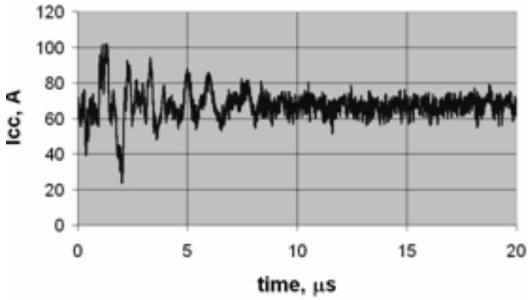


Figure 9: Icc on EV7 chip running code SWIM.

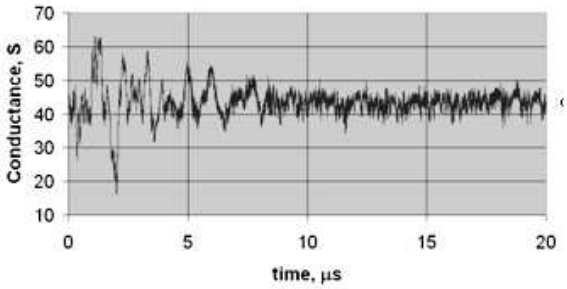


Figure 10: Equivalent conductance variation on EV7 chip running power virus SWIM.

7. Conclusion

There are no direct methods of measurement of PDS current on functioning die. Current can be extracted indirectly from measured Vcc if PDS impedance is known. Measurements of PDS impedance, in turn, requires

knowledge of PDS current. The solution we suggested is to generate a step-wise computer process and predict PDS current for this process using equivalent conductance representation of a chip. Equivalent conductance can serve as a quantification of chip switching activity. PDS current and chip activity for any computer process can be determined by de-convolution involving measured Vcc and known PDS impedance. The measurement are easy to perform because only Vcc on-die and current on voltage regulator are measured directly so we can avoid calibration and compensation that are most challenging parts for conventional measurement techniques. The proposed methodology is the only available methodology for measurement PDS current and activity variations on a functioning chip

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High Speed and Low Noise Packaging Design Methodologies for 40 Gbps SerDes Channel with PBGA Type Package

D. G. Kam[1], **J. Yu**[2], **H. Choi**[2], **K. Bae**[2], **J. Kim**[3], **D.-K. Jeong**[3], **C. Lee**[2], **and J. Kim**[1]

[1]Korea Advanced Institute of Science and Technology (KAIST), Korea
[2]Amkor Technology Korea, Korea
[3]Seoul National University, Korea

A 40 Gbps package solution that uses merely cheap wire-bonding plastic ball grid array (PBGA) technology is presented. Since such a high speed is well beyond the reach of conventional package designs, a number of techniques are devised to achieve the bandwidth for transmitting a 40 Gbps NRZ bit stream with a single differential channel: to shorten the bonding wires for critical signals even by cutting power/ground rings partially, to use low-loss RF substrate, to prohibit return current from transitioning layers by modifying conventional stack up and ball distribution, to use shielding structure for critical signals, and to remove some balls to reduce the length of 40 Gbps channel on a package. The effect of each technique is examined quantitatively by simulation and measurement, from which some of the techniques described above are adopted. The package type is determined as four-layer wire-bonding PBGA that also accommodates on-package decoupling capacitors for power integrity and a heat slug for thermal dissipation. Post-layout full wave simulation shows considerable possible improvement of channel performance. A prototype package is fabricated by Amkor Technology Korea. A test board is also fabricated by using low-loss PTFE material. The insertion loss of the overall channel is measured to be less than 3 dB up to 40 GHz. Finally the eye-diagram measured on the test board verifies the proposed techniques to be working solution of high speed and low noise package design for 40 Gbps SerDes channel with PBGA type package.

3D-SOP Millimeter-wave Functions for High Data Rate Wireless Systems Using LTCC and LCP Technologies

J.-H. Lee, **D. Thompson**, **S. Pinel**, **J. Papapolymerou**, **and M. M. Tentzeris**
Georgia Institute of Technology, USA

Millimeter-wave (mmW) electronics for commercial applications, such as short-range broadband wireless communications and automotive collision avoidance radars, require low-manufacturing cost, excellent performance, and high level of integration. The multilayer LTCC System-On-Package (SOP) approach is very well suited for these requirements because it offers a great potential for passives' integration and enables microwave devices to be fabricated with high reliability, while maintaining the low cost. The very mature multilayer fabrication capabilities of LTCC up to 100+ GHz enable the replacement of broadside coupling by vertical coupling and make LTCC a competitive solution to meet millimeter wave design requirements. As an alternative, Liquid Crystal Polymer (LCP) is an organic material that offers a unique low-cost all-in-one solution for high frequency designs due to its ability to act as both a high-performance flexible substrate ($\varepsilon_r = 2.9-3.1, \tan\delta = 0.002-0.004$) and a near-hermetic package for multilayer modules. These characteristics make LCP very appealing for many applications and it can be viewed as a prime technology for enabling system-on-package RF and mmW designs. In this paper, we present the development of various advanced 3-D LTCC and LCP system-on-package architectures enabling a complete passive solution for compact, low cost wireless front-end systems to be used in RF and mmW frequency ranges. The 3D embedded functions, which have been developed, include slotted patch resonator filters for achieving compactness and great compromise between size and power handling and directional filters to provide easy and compact solutions for different applications, such as mixing and multiplexing.

One important function that can be easily integrated in multilayer modules is filtering. In order to maintain their properties in compact topologies, band pass filters are commonly realized using slotted patch resonators in mmW frequencies due to their miniaturized size, the great compromise between size and power handling and their easy-to-design layout. In this paper, one single mode slotted patch filter (1-pole) with a transverse cut on each side has been designed and embedded in LTCC ($\varepsilon_r = 5.4, \tan\delta = 0.0015$) for 38–40 GHz applications such as vehicular communications. The patch filter (1.02 mm × 1.02 mm) has been optimized in aim of 6.5% bandwidth, 39 GHz center frequency, and < 3 dB insertion loss. Such a structure has been developed from the commonly used half-wavelength square patch at 39 GHz by adding one transverse cut on each side leading to a significant reduction of the patch size and a good power handling. The desired coupling coefficients are obtained by inserting the feedlines and the single resonator into different metal layers. The stripline filters are excited through vias connecting the top metal with the next underlying metal, enabling the package to prevent radiation loss. The experimental results of the filter agree very well with simulation data, demonstrating a minimum insertion loss of 2.3 dB, the return loss > 18.2 dB over pass band, and bandwidth about 6.4%.

The LCP filter design we developed exploits the ripple near the cut off frequency of a Tchebyscheff low pass filter to create a band pass response. The initial low pass filter has been implemented by cascading two low impedance sections. Two slots have been added in each of these low impedance sections to enhance the ripple amplitude, and a ripple of 10 dB in amplitude has been measured. Then an open stub creating a transmission zero at 36 GHz has been added to enhance the rejection up to -35 dB in the lower band. Capacitive feeding can be used to remove the low frequency pass band if it is required resulting in a pass-band response centered at 60 GHz and a relative 3 dB bandwidth of 15% with minimum insertion losses as low as -1.5 dB. A ripple of $+/-0.15$ dB has been measured over a bandwidth of 6 GHz centered at 60 GHz.