A New Generalized Space Vector Modulation Algorithm for Neutral-point-clamped Multilevel Converters

P. Purkait and R. S. Sriramakavacham
Birla Institute of Technology, India

Abstract—Neutral-point-clamped converters are increasingly applied in industrial drive systems as they allow the use of lower voltage devices in higher voltage applications, provide reduced output voltage total harmonic distortion(THD), and can develop low common mode voltage. Several distinct modulation strategies have been proposed in the past for eliminating the common mode voltage, providing low THD output voltage or reducing the neutral point current ripple. However each of these strategies improves the performance of the converter in one view point while losing performance in the other view point. A new generalized space vector modulation technique is proposed. Analytical model and simulation results are presented.

1. Introduction

In recent years, industry has begun to demand higher power equipment, which now reaches the megawatt level. Controlled ac drives in the megawatt range are usually connected to the medium voltage network. Today it is hard to connect a single power semiconductor switch directly to medium voltage grids. For these reasons, a new family of multilevel inverters came as the solution for working with higher voltage levels. In particular, they provide low line voltage dv/dt and improved spectral characteristics of the output signals. The three level neutral-point-clamped (NPC) converters are used widely in adjustable speed a.c drive systems, providing less stress on motor winding, insulation and bearings. It is leading to an increase of the reliability and the life period of the drive systems.

Several carrier-based and space vector modulation strategies have been proposed for these converters [7]. These algotithms were designed to provide adjacent state switching action in the converter which yields the lowest possible output voltage and current total harmonic distortion. The most significant advantages of SVPWM are fast dynamic response and wide range of fundamental voltage compared with the conventional PWM. But when it is applied to the diode-clamped converter, the SVPWM strategy also has to solve the neutral-point voltage un-balance problem.

There are three main steps to obtain the proper switching states during each sample period for the SVPWM method:

1. Choose proper basic vectors.
2. Calculation of dwelling time of selected vectors.
3. Selection of proper sequence of pulses.

One way for calculating the time is to decompose all the vectors into real and imaginagy part [1]. Another way is to calculate the time according to reference voltage vector of each phase [3, 2].

To solve the problem of computational complexity in multilevel converter due to large number of redundant switching states, a new generalized space vector algorithm is proposed. This new space vector strategy eliminates low frequency ripple from the dc link capacitors of a three-level converter. The proposed algorithm for threeClevel converter is verified by simulation and the results are compared with the existing method, nearest three vector algorithm [4].

2. Three-phase Three-level Converter

Figure 1 presents the basic structure of a three-level neutral-point-clamped converter. Each of three legs of the converter consists of four power switches, four freewheeling diodes and two clamping diodes that limit the voltage excursions across each device to half the input dc-bus voltage.

3. Nearest Three Vector Modulation

Table 1 shows the possible switching states for the three level converter of Figure 1. There are nineteen basic space vectors for a three-level converter and they are shown in Figure 2. The zero voltage vector has three switching states (000, 111, -1-1-1). Each of the six small vectors (V_1–V_6) has two switching states and each of the middle vectors (V_8, V_{10}, V_{12}, V_{14}, V_{16}) and the large vectors (V_7, V_9, V_{11}, V_{13}, V_{15}, V_{17}) has one state respectively.

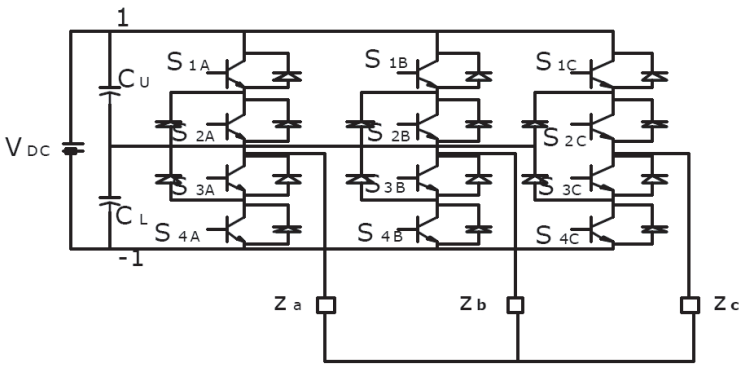

Figure 1: Basic structure of three level diode clamped converter.

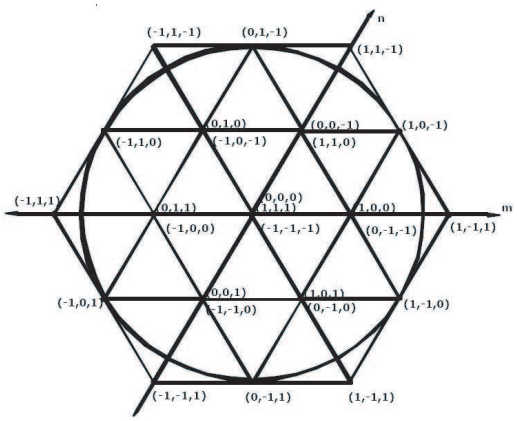

Figure 2: Switching states of converter.

Table 1: Switching states of three-level converter ($X = A, B, C$).

STATUS	S_{1X}	S_{2X}	S_{3X}	S_{4X}
1	ON	ON	OFF	OFF
0	OFF	ON	ON	OFF
-1	OFF	OFF	ON	ON

In SVPWM technique, the reference voltage vector V_r is located in a triangle, in which three voltage vectors are corresponding to the three apexes. They are selected to minimize the harmonic components of the output line voltage.

The dwelling time of each vector should satisfy the following equations:

$$V_1 t_1 + V_7 t_7 + V_8 t_8 = V_r T \quad (1)$$

$$t_1 + t_8 + t_8 = T \quad (2)$$

where T is the sampling period and t_1, t_7 and t_8 are the dwelling time of V_1, V_7 and V_8 respectively.

Following four methods are required in the nearest three vector modulation algorithm to attain the complete switching states for a multilevel converter by using SVPWM.

Step I: Decomposing of Basic Vectors

A new coordinates namely *m-n* coordinates can be established. The new coordinate have two axes intersecting with the angle of $\pi/3$. Only the first quadrant of the coordinate is used because the vector located in other region can be transformed to the first quadrant by clockwise rotating an angle $K^*(\pi/3)$ where, $K = 1, 2, 3, 4, 5$ for region B, C, D, E and F respectively.

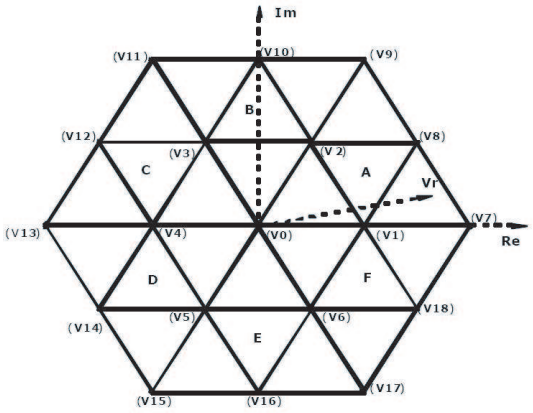

Figure 3: Space vector of the three level converter.

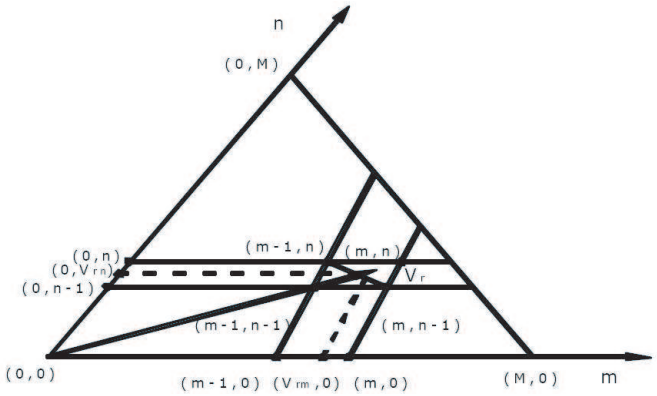

Figure 4: Decomposing of reference vector.

Universally a $(M+1)$ level inverter is discussed here. As shown in Figure 4, the reference vector is decomposing into m-axis and n-axis.

$$V_{rm} = 2MV_r/(\sqrt{3}V_{dc})\sin(\pi/3-\theta) \quad (3)$$

$$V_{rn} = 2MV_r/(\sqrt{3}V_{dc})\sin(\theta) \quad (4)$$

Step II : Selecting Three Nearest Vectors

Considering that following inequalities are satisfied by V_{rm} and V_{rn}

$$(m-1) < V_{rm} < m \quad (5)$$

$$(n-1) < V_{rn} < n \quad (6)$$

where m and n are integers. There are three possible cases:

1. $V_{rm}+V_{rn} < (m+n-1)$: That means V_r is located in the left bottom shadow triangle. The vectors $(m-1,n-1)$, $(m-1,n)$ and $(m,n-1)$ are the nearest vectors.
2. $V_{rm}+V_{rn} > (m+n-1)$: That means V_r is located in the right top shadow triangle. The vectors $(m-1,n)$, $(m,n-1)$ and (m,n) are the nearest vectors.
3. $V_{rm}+V_{rn} = (m+n-1)$: V_r lies at the middle line and either 1. or 2. can be choosen.

Step III : Dwelling Time Calculation

Dwelling time calculation is given here. Taking $(m1,n1)$, $(m2,n2)$ and $(m3,n3)$ are three nearest vector. Corresponding dwelling time can be calculated from the following equations.

$$m_1t_1+m_2t_2+m_3t_3 = V_{rm}*T \quad (7)$$

$$n_1t_1+n_2t_2+n_3t_3 = V_{rn}*T \quad (8)$$

$$t_1+t_2+t_3 = T \quad (9)$$

Step IV : Neutral Point Potential Control

It is very important to balance neutral point potential. For balancing neutral point potential selection of proper switching sequence is necessary. For example, when V_r falls in the triangle formed by the apexes of vectors V_1, V_7 and V_8, the switching sequence can be selected as (100) - (10-1) - (00-1) - (0-1-1) or (110) - (100) - (10-1) - (00-1). The two sequences lead to the same output voltage but have the opposite effect on the neutral point voltage.

Over Modulation Control

However, there is one exception when the reference voltage vector lies outside the hexagon. In this case, the over modulation mode occures and the output line voltages distort.

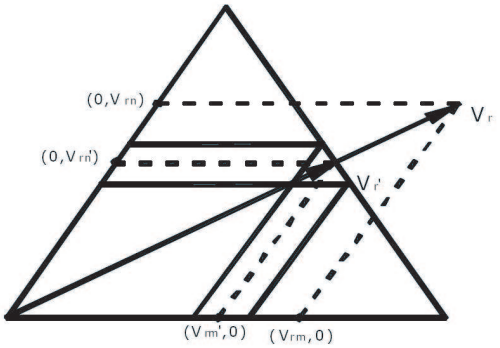

Figure 5: Over modulation control.

Following algorithm can be used when reference vector lies in the over modulation region,

$$\text{If } (V_{rm}+V_{rn}) > M$$

$$V_{rm'} = V_{rm}*M/(V_{rm}+V_{rn}) \quad (10)$$

$$V_{rn'} = V_{rn}*M/(V_{rm}+V_{rn}) \quad (11)$$

4. New Space Vector Modulation Algorithm

It has been shown that switching states where the three ac terminals are connected to the three different voltage level of dc bus are the primary cause of increased harmonic content in the dc bus currents. The presence of significant third harmonic content in the neutral point current causes a significant sizing penalties on the dc link capacitor of three level converter [6]. A new space vector modulation algorithm is proposed to eliminate the harmonic content in neutral current.

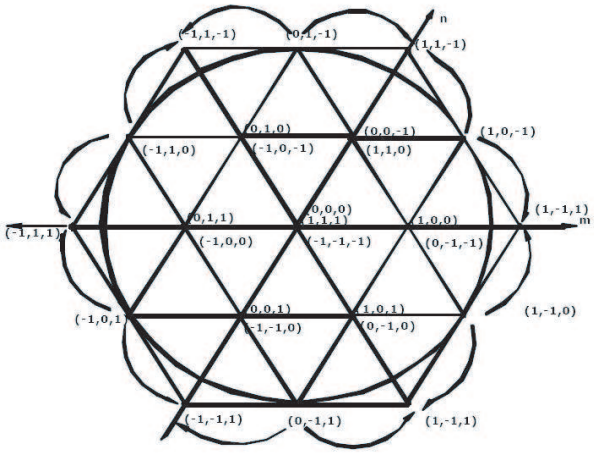

Figure 6: Redistribution of switching states in R.S.S. algorithm.

It can be deduced that the identical voltages can be generated if the duty cycle of these state is equally divided between two states that are adjacent to it and lie on the same hexagonal plane. Figure 6 shows the redistribution of switching states.

As an example, redistribution of dwelling time in Figure 6 for (1,-1,-1), (1,1,-1) and (1,0,-1) can be done as follows,

$$t_{1,-1,-1} = t_{1,-1,-1} + (t_{1,0,-1}/2) \tag{12}$$

$$t_{1,1,-1} = t_{1,1,-1} + (t_{1,0,-1}/2) \tag{13}$$

$$t_{1,0,-1} = 0 \tag{14}$$

Though we have eliminated six switching states still DC-bus utilization factor in this method is identical with nearest three vector modulation, as the hexagon and inscribe circle are equal.

5. Simulation Results

Extensive MATLAB/SIMULINK models of three level inverter systems were developed for analysing the nearest three point modulation and new proposed method on output line voltage and neutral point current.The simulation of threeClevel converter shown in Figure 1 was done under the conditions listed in Table 2.

Table 2: Simulation conditions.

Sampling Time	50 μSec.
DC Link Voltage	400 Volts
Active Load	1 KW
Reactive Power (-ve)	500 VAR
Output Frequency	50 Hz
Modulation Index	0.7

1. Output Line Voltage

Figure 7 and Figure 9 are the line-line voltage of nearest three vector modulation and new proposed approach respectively. The FFT analysis (Figure 8 and Figure 10) of both the line-line voltages are also shown.

2. Line Current

Figure 11 and Figure 13 are the line currents of nearet three vector modulation and new proposed approach respectively and their FFT analysis also shown in Figure 12 and Figure 14.

3. Neutral Point Current

FFT analysis of neutral current of nearet three vector modulation and new proposed approach are shown in Figure 15 and Figure 16 respectively. New proposed method eliminates the harmonic content in neutral point current while the nearest three vector method shows harmonics in neutral point current.

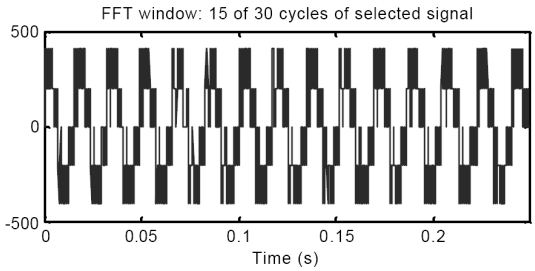

Figure 7: Line-line voltage.

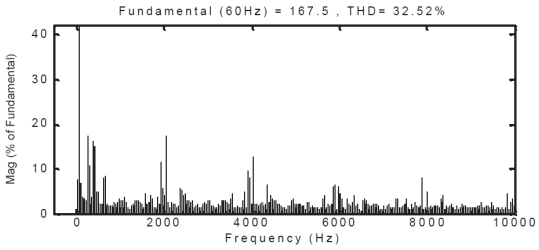

Figure 8: FFT analysis of line-line voltage.

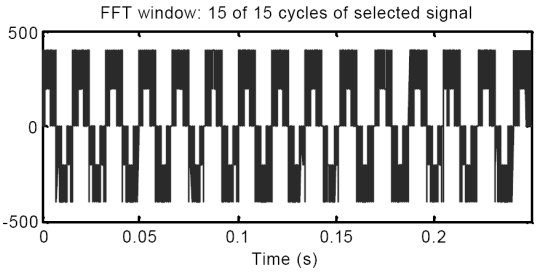

Figure 9: Line-line voltage waveform.

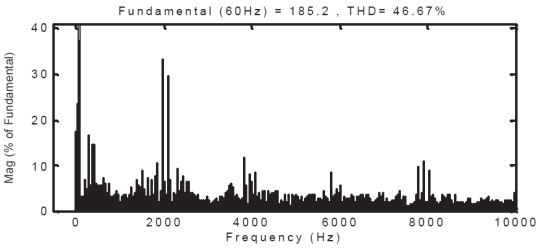

Figure 10: FFT analysis of line-line voltage.

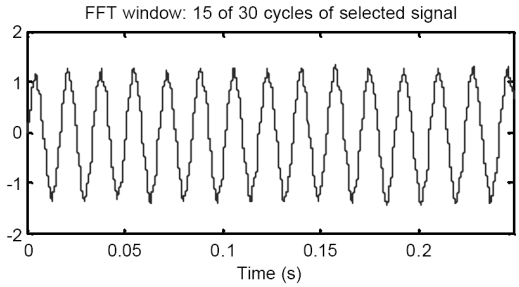

Figure 11: Line current waveform.

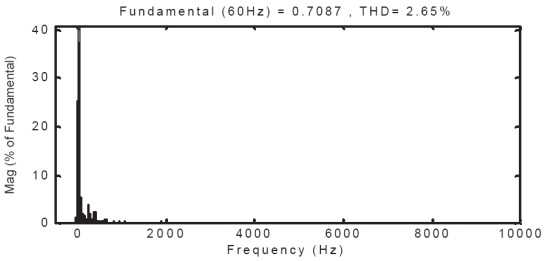

Figure 12: FFT analysis of line current.

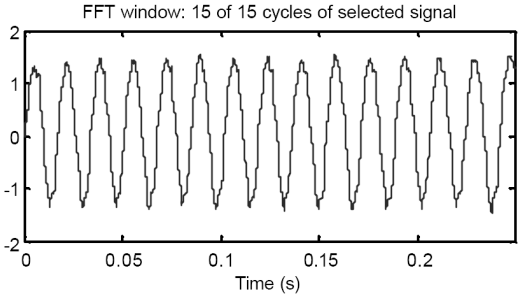

Figure 13: Line current waveform.

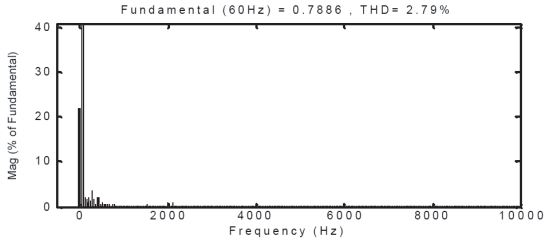

Figure 14: FFT analysis of line current.

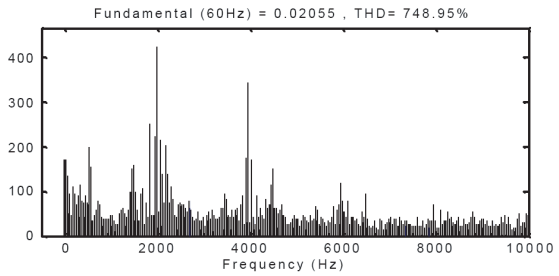

Figure 15: FFT analysis of neutral current.

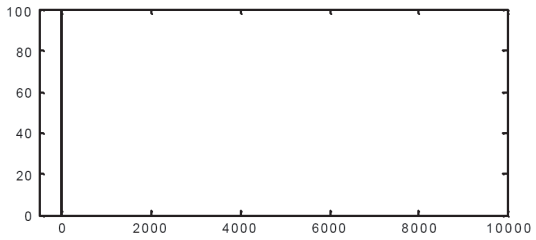

Figure 16: FFT analysis of neutral current.

6. Conclusion

A new simple SVPWM method is proposed and verified by simulation of three-level-inverter. If number of levels increases more complexity will come in the proposed method while algorithm will be same. This paper presents a new way of implementing the proposed space vector modulation algorithm for reducing the neutral point current in the multilevel inverter.

From the FFT analysis of line voltage and neutral current it is concluded that

1. Low frequency harmonic content of the neutral current is zero.
2. Neutral point current has a zero d.c average value.
3. Line voltage contains slightly larger harmonics in proposed method with respect to nearest three vector modulation.

REFERENCES

1. Seo, J. H., C. H. Choi, and D. S. Hyun, "A new simplified space-vector PWM method for three-level-inverters," *IEEE Trans. Power Electronics*, Vol. 16, 527–534, July 2001.
2. Maruyama, T., M. Kumano, and M. Asish, "A new asynchronous PWM method for a threelevel-inverter," *Conf. Rec. 1991 IEEE Int. Power Electronics Specialists Conf.*, 366–371, 1991.
3. Seo, J. H. and C. H. Choi, "Compensation for the neutral-point-potential variation in three-level-space-vector PWM," *Conf. Rec. 2001 IEEE Int. Applied Power Electronics Conference and Exposition*, Vol. 2, 1135–1146, 2001.
4. Hu, L., H. Y. Wang, Y. Deng, and X. N. He, "A simple SVPWM algorithm for multilevel inverters," *2004 35th Annual IEEE Power electronics Specialist Conference*, 3476–3480, 2004.
5. Bendre, A., S. Krstic, J. V. Meer, and G. Venkataramanan, "Comparative evalution of modulation algorithms for neutralpoint-clamped converters," *IEEE Transaction on Industry Applications*, Vol. 41, No. 2, March/April 2005.
6. Bendre, A. and G. Venkataramanan, "Radial space vector modulation—a new space vector technique for reducing dc link capacitor harmonic currents in three-level-converters," *Conf. Rec. IEEE-IAS Annu. Meeting*, Vol. 1, 684–691, 2003.
7. Rodviger, J., J.-S. Lai, and F. Z. Leng, "Multilevel inverters, control and applications," *IEEE Trans on Industrial Electronics*, Vol. 49, No. 4, 724–738, August 2002.