A Single Phase Single Stage AC/DC Converter with High Input Power Factor and Tight Output Voltage Regulation

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Abstract—A single stage single switch AC/DC converter is an integration of input current shaper and a DC/DC cell with a shared controller and one active switch. The converter is applicable for digital input power supply with high input power factor and tight output voltage regulation. The focus of the topology is to reduce the DC bus voltage at light load without compromising with input power factor and voltage regulation. The concept behind this topology is direct power transfer scheme. Using special configuration of DC/DC cell does reduction of DC bus voltage and DC/DC cell works on the principle of series charging and parallel discharging. The power output of this converter can go up to 200 W.

1. Introduction

An ac to dc converter is an integral part of any power supply unit used in the all electronic equipments. Also, it is used as an interface between utility and most of the power electronic equipments. These electronic equipments form a major part of load on the utility. Generally, to convert line frequency ac to dc, a line frequency diode bridge rectifier is used. To reduce the ripple in the dc output voltage, a large filter capacitor is used at the rectifier output. But due to this large capacitor, the current drawn by this converter is peaky in nature. This input current is rich in low order harmonics. Also, as power electronics equipments are increasingly being used in power conversion, they inject low order harmonics into the utility. Due to the presence of these harmonics, the total harmonic distortion is high and the input power factor is poor. Due to problems associated with low power factor and harmonics, utilities will enforce harmonic standards and guidelines which will limit the amount of current distortion allowed into the utility and thus the simple diode rectifiers may not in use. So, there is a need to achieve rectification at close to unity power factor and low input current distortion. Initially, power factor correction schemes have been implemented mainly for heavy industrial loads like induction motors, induction heating furnaces etc., which forms a major part of lagging power factor load. However, the trend is changing as electronic equipments are increasingly being used in everyday life nowadays. Hence, PFC is becoming an important aspect even for low power application electronic equipments.

The objective of the paper has been in the direction of better understanding of direct power transfer scheme, closed loop simulation and analysis of proposed AC/DC converter. Emphasis of the paper has been the design of 100 W AC/DC converter with high input power factor and tight output voltage regulation without compromising with high DC bus voltage at light loading condition.

2. Power Factor Correction Techniques

In recent years, single-phase switch-mode AC/DC power converters have been increasingly used in the industrial, commercial, residential, aerospace, and military environment due to advantages of high efficiency, smaller size and weight. However, the proliferation of the power converters draw pulsating input current from the utility line, this not only reduce the input power factor of the converters but also injects a significant amount of harmonic current into the utility line [1]. To improve the power quality, various PFC schemes have been proposed. There are harmonic norms such as IEC 1000-3-2 introduced for improving power quality. By the introduction of harmonic norms now power supply manufacturers have to follow these norms strictly for the remedy of signal interference problem [2].

The various methods of power factor correction can be classified as:

(1) Passive power factor correction techniques
(2) Active power factor correction techniques

In passive power factor correction techniques, an LC filter is inserted between the AC mains line and the input port of the diode rectifier of AC/DC converter as shown in Figure 1. This technique is simple and rugged but it has bulky size and heavy weight and the power factor cannot be very high [1]. Therefore it is now not

applicable for the current trends of harmonic norms. Basically it is applicable for power rating of lower than 25 W. For higher power rating it will be bulky.

In active power factor correction techniques approach, switched mode power supply (SMPS) technique is used to shape the input current in phase with the input voltage. Thus, the power factor can reach up to unity. Figure 2 shows the circuit diagram of basic active power correction technique [2]. By the introduction of regulation norms IEC 1000-3-2 active power factor correction technique is used now a day. There are different topologies for implementing active power factor correction techniques. Basically in this technique power factor correcting cell is used for tracking the input current in phase of input voltage such that input power factor come up to unity. Comparing with the passive PFC techniques, active PFC techniques have many advantages such as, high power factor, reduced harmonics, smaller size and light-weight. However, the complexity and relatively higher cost are the main drawbacks of this approach.

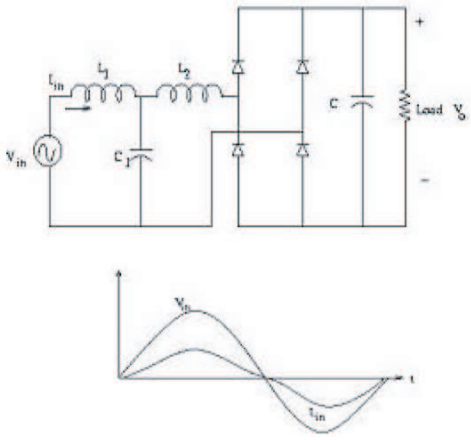

Figure 1: Passive PFC technique.

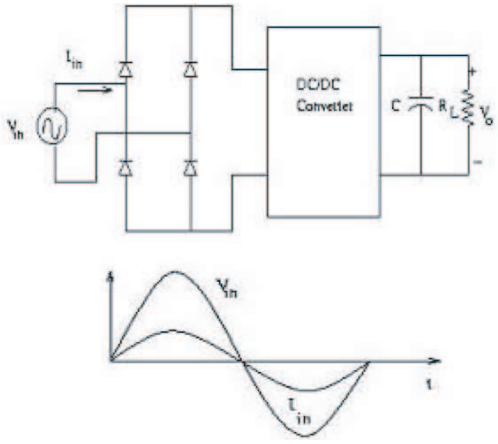

Figure 2: Active PFC technique.

The active PFC techniques can be classified as:

(1) PWM power factor correction techniques

(2) Resonant power factor correction techniques

(3) Soft switching power factor correction techniques

In PWM power factor correction approach, the power switching device operates at pulse-width-modulation mode. Basically in this technique switching frequency of active power switch is constant, but turn-on and turn-off mode is variable. The advantages are simple configuration, ease of analysis and control, lowest voltage and current stress. Therefore it is extensively used in PFC circuits. For the minimization of converter size PWM technique generates significant switching loss [1].

Different topologies of PWM techniques are as follows:

(1) Buck type

(2) Flyback type

(3) Boost type

(4) Cuk' type

Figure 3 shows the buck type topology. The advantage of buck type topology is that the converter can supply a low output voltage with respect to input voltage. The disadvantages are, significant current distortion, EMI is higher because discontinuous input current so filter design is costly. It is a basic DC-DC converter and it is not used for power factor correction [1].

Figure 4 shows the flyback type topology. Its advantages are, output voltage can be higher or lower than input voltage and input and output can be isolated. The disadvantages are higher switching device voltage and current rating, input current is discontinuous so requirement of careful design of input filter, difficult to program the input current with current mode control [1].

The boost type topology is shown in Figure 5. Advantages of this topology are current mode control is easy and less EMI so reduced input filtering requirements. The main disadvantages are more conduction loss, no isolation and output voltage is always higher than input voltage [1].

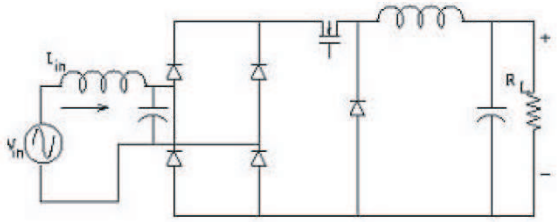

Figure 3: Buck type topology.

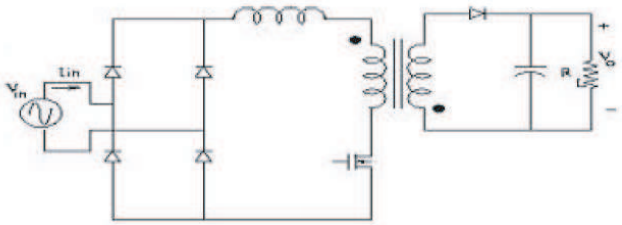

Figure 4: Flyback type topology.

The Cuk' type is shown in Figure 6. The advantages are, input current is remain continuous even if the converter operates in discontinuous conduction mode, and output voltage can be lower or higher than the instantaneous input voltage. The disadvantages are the increased voltage and current stress on power devices, requirement of extra inductor and capacitor and isolation is not provided [1].

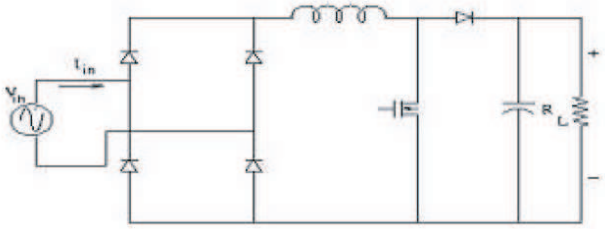

Figure 5: Boost type topology.

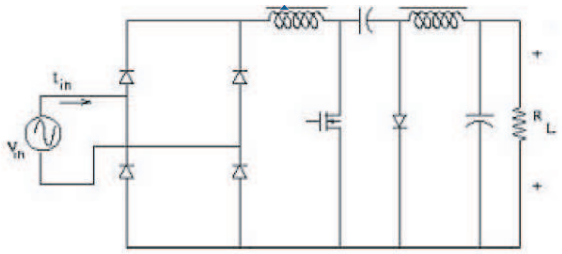

Figure 6: Cuk' type topology.

In the resonant converter, the voltage across a switch or the current through a switch is shaped by the resonance of inductor and capacitor to become zero at the time of turned on or off. Thus the switching loss is greatly reduced. The high power factor is achieved by the natural gain-boosting characteristic of the resonant converter. The major drawbacks are higher voltage and current stress on the power switch with respect to PWM mode and variable switching frequency employed. Figure 7 shows a PFC circuit in which a resonant converter is inserted between the input diode rectifier and the dc-dc converter. This resonant converter can be series resonant converter or a charge pump resonant network [3]. The advantage is that the current stress and voltage stress on resonant components as well as power switches are lower than the previous resonant converter [1].

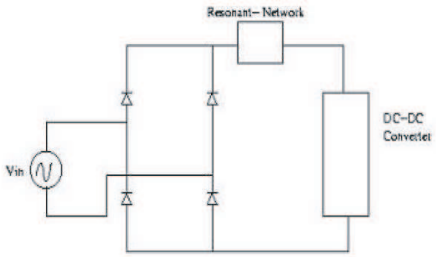

Figure 7: Resonating PFC circuit.

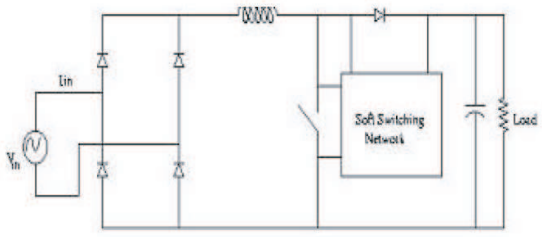

Figure 8: Soft switching PFC circuit.

The soft-switching PFC technique combines the advantages of PWM mode and resonant mode techniques with an additional resonant network consisting of a resonant inductor, a resonant capacitor and an auxiliary switch. The AC/DC converter operates in PWM mode during most portion of a switching cycle but operates in resonant mode during the switch turn-on and turn-off intervals. As a result, the PFC circuit works at constant switching frequency and the power switch turns on and off at zero current or zero voltage conditions. Thus efficiency and power factor both improved by this technique. Figure 8 shows boost PFC circuit with a soft switching network [1].

3. Single Phase Active Power Factor Correction

Conventional off-line power converters with diode capacitor rectifier front-end have distorted input cur-

rent waveform with high harmonic content. They cannot meet neither the European line-current harmonic regulations defined in the IEC1000-3-2 document nor the corresponding Japanese input-harmonic current specifications. To meet the requirements of above norms it is customary to add a power factor corrector ahead of the isolated dc/dc converter section of the switching power supply. Again another dc/dc converter is needed for output voltage regulation. Thus there are two converter is needed for single-phase active power factor correction for the requirement of high input power factor and tight output regulation. There are two approaches for single-phase active power factor correction:

(1) Two-stage approach

(2) Single-stage approach

Two-stage approach is commonly used approach in high power applications [4]. The block diagram of two stages PFC converter is shown in Figure 9. In this approach, there are two independent power stages. The front-end PFC stage is usually a boost or buck-boost (or flyback) converter. The dc/dc output stage is the isolated output stage that is implemented with at least one switch, which is controlled by an independent PWM controller to tightly regulate the output voltage. The two-stage approach is a cost-effective approach in high power applications; its cost-effectiveness is diminished in low-power applications due to the additional PFC power stage and control circuits.

A single-stage scheme combines the PFC circuit and dc/dc power conversion circuit into one stage. A number of single-stage circuits have been reported in recent years. Figure 10 shows the block diagram of single-stage approach. Compared to the two-stage approach, the single approach uses only one switch and controller to shape the input current and to regulate the output voltage. Although for a single-stage PFC converter attenuation of input-current harmonics is not as good as for the two-stage approach. But it meets the requirements of IEC1000-3-2 norms. Again it is cost effective and compact with respect to two stage approach [4].

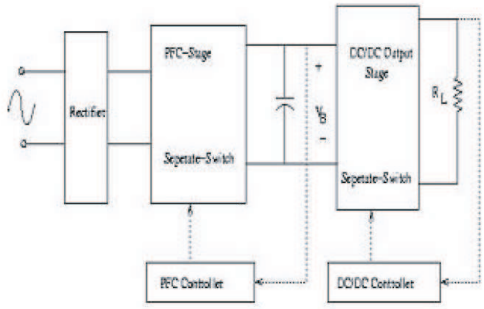

Figure 9: Block diagram of two stage approach.

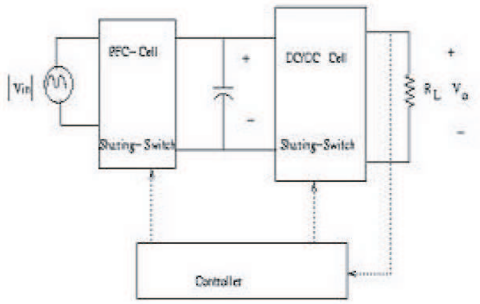

Figure 10: Block diagram of single stage approach.

There are four possible combinations to obtain different single stage single switch PFC converters [5]:

(1) Discontinuous Conduction Mode PFC + Continuous Conduction Mode DC/DC

(2) Discontinuous Conduction Mode PFC + Discontinuous Conduction Mode DC/DC

(3) Continuous Conduction Mode PFC + Continuous Conduction Mode DC/DC

(4) Continuous Conduction Mode PFC + Discontinuous Conduction Mode DC/DC

4. Direct Power Transfer Scheme

Either in two-stage or single-stage of single phase PFC the input power is processed twice to reach the output. There are two functional cells known as PFC cell and DC/DC cell is used for power factor correction and output voltage regulation respectively. Figure 11 shows the power processing in typical single-phase single-stage approach by block diagram. Suppose efficiency of PFC cell is η_1 and DC/DC cell is η_2 than the output power will be

$$P_0 - P_{\text{in}}\eta_1\eta_2 \tag{1}$$

Thus the efficiency of single-stage AC/DC converter will be,

$$\eta = \eta_1\eta_2 \tag{2}$$

Thus the twice power processing approach means low conversion efficiency because it is a product of two fraction. So, advancement is needed for the improvement of conversion efficiency.

The proposed approach come into picture according to that, it is not necessary to process all input power twice to achieve well-regulated and high input power factor DC output power. In this approach some power is

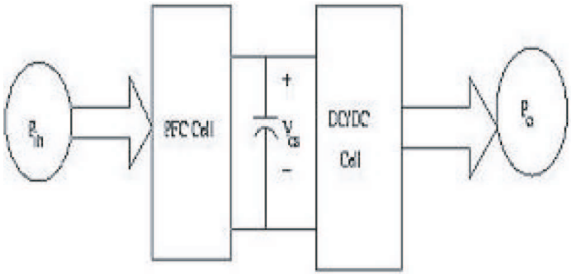

Figure 11: Conventional single stage approach.

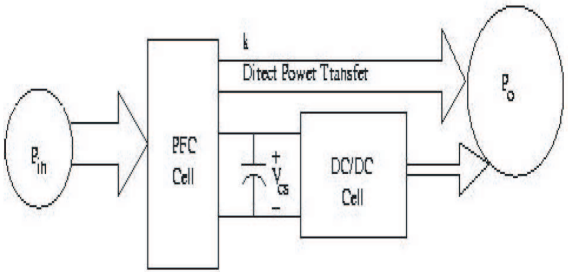

Figure 12: Proposed DPT scheme.

processed only once and remaining power processed twice to keep the total DC output power constant. Figure 12 shows the proposed new direct power transfer scheme. For this kind of power transfer, with whom some power is processed only once is called direct power transfer (DPT) scheme [6].

Let k portion of power from PFC cell be directly transferred to output, and remaining (1-k) power from PFC cell is stored in intermediate bus capacitor and then processed by DC/DC cell. Based on the proposed concept, output power can be obtained by Eq. (4), (3).

$$P_0 = P_{\text{in}}\eta_1\eta_2(1-k) + P_{\text{in}}\eta_1 k \tag{3}$$

Thus efficiency of proposed direct power transfer scheme single-stage PFC AC/DC converter is,

$$\eta = \eta_1\eta_2 + k(1-\eta_2)\eta_1 \tag{4}$$

Comparing Eq. (2) and Eq. (4), it is easy to say efficiency of DPT scheme is more than the efficiency of conventional single-stage scheme.

5. Direct Power Transfer Topology

The proposed DPT topology integrates flyboost PFC cell in existing single stage DC/DC cell. All the derived topologies are differentiated by only application of DC/DC cell. Different DC/DC cells are used for improving voltage regulation and reducing DC bus stress. Power unbalance between PFC stage and dc/dc stage is the inherent reason for causing high DC bus voltage stress. In order to meet the criteria of low DC bus voltage DC/DC cell used in this converter is work on the concept of "series charging, parallel discharging capacitors scheme (SCPDC)" [5]. The SCPDC means that the two energy-storage capacitors are charged in series when the switch is off and discharged in parallel when switch is on.

This topology integrates one parallel PFC cell and one parallel-series forward DC/DC conversion cell. Parallel PFC cell is basically a flyback transformer and integration of boost features. For achieving high power factor PFC block should work on DCM. Figure 13 shows the laboratory type AC/DC converter. Flyboost part is already explained in section 4.2. Here main difference in flyboost part of previous topology is unbalanced power is controlled properly, so DC bus voltage is less compared to other topologies of single stage single switch AC/DC converter.

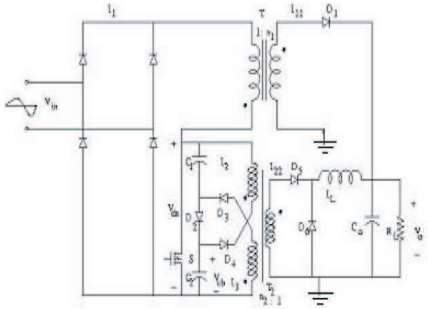

Figure 13: Proposed AC/DC converter.

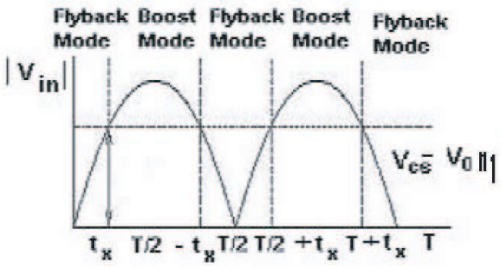

Figure 14: Modes of operation.

Parallel PFC cell contains; transformer T_1, input bridge rectifier, two intermediate bus capacitors, diode D_1 and diode D_2, and active switch S. The parallel-series forward DC-DC conversion cell contains, forward transformer T_2, output inductor L_o, output capacitor C_o, and also bus capacitors, diodes, switch. Thus both cells share bus capacitors, the only active switch and controller. Same as other single-stage PFC topologies the two cells are operate independently. But the operation of this topology differs in other topologies in terms of

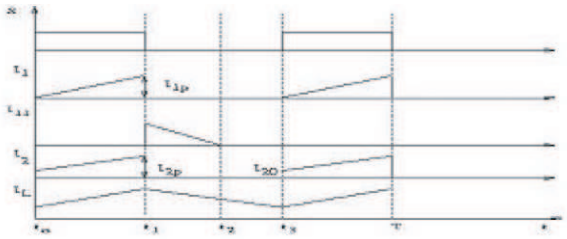

Figure 15: Flyback mode of operation.

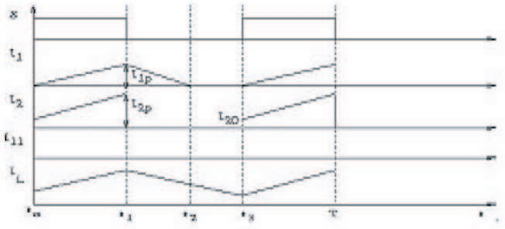

Figure 16: Boost mode of operation.

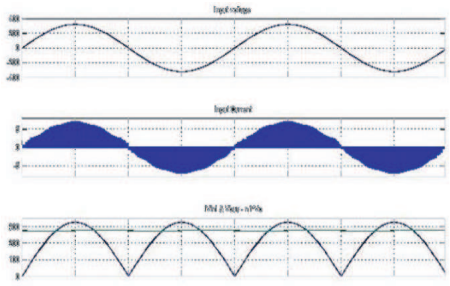

Figure 17: Waveforms of input voltage, input current and modes of operation.

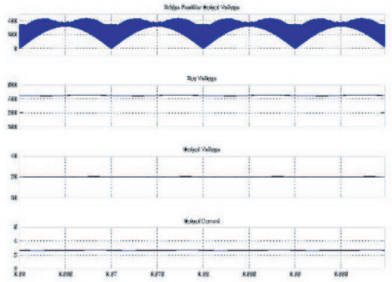

Figure 18: Waveforms of bus voltage, output voltage and current.

parallel power flow nature and special mode of operation. For low input voltage, works as a flyback transformer and at the high input voltage works as a boost inductor.

Modes of Operation: PFC cell works in two modes of operation. The following discussion explains the modes of operation.

Suppose diode D_1 is conducting, applying KVL for primary side

$$|V_{\text{in}}(t)| = V_o/n_1 + V_{D2} + V_{cb}$$

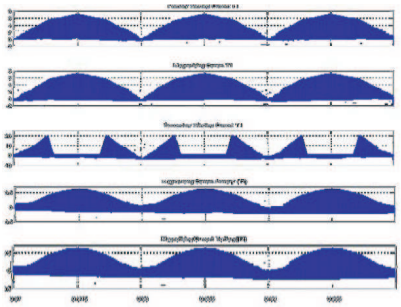

Figure 19: Waveforms of current of transformer T_1 and T_2.

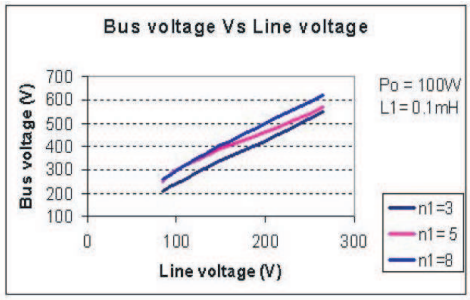

Figure 20: Bus voltage versus line voltage.

Where $V_{\text{in}}(t)$, is input voltage, V_o the output voltage, n_1 the turn ratio of transformer T_1, V_{cb} the voltage across bus capacitor and V_{D2} the voltage across diode D_2.

So, $V_{D2} = |V_{\text{in}}(t)| - (V_{cb} - V_o/n_1)$

For D_2 to be conducting the condition is;

$$|V_{\text{in}}(t)| \geq (V_{cb} - V_o/n_1) \tag{5}$$

Now suppose diode D_2 is conducting, the reflected voltage on secondary side will be;

$$[|V_{\text{in}}(t)| - V_{cb}]n_1$$

Applying KVL on secondary side

$$[|V_{\text{in}}(t)| - V_{cb}]n_1 + V_{D1} + V_o = 0$$

Where, V_{D1} is the voltage across diode D_1. For D_1 to be conduct V_{D1} should be greater or equal to zero, so the condition is;

$$|V_{\text{in}}(t)| \leq (V_{cb} - V_o/n_1) \tag{6}$$

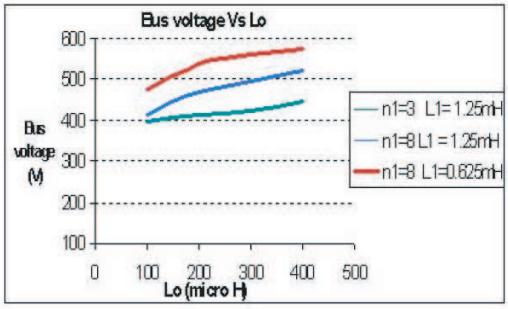

Figure 21: Bus voltage versus output inductance.

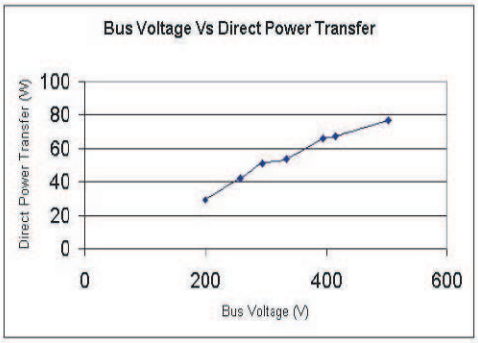

Figure 22: Bus voltage versus DPT.

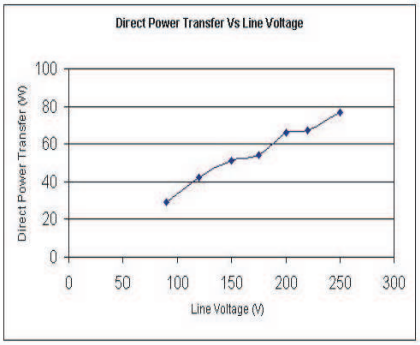

Figure 23: DPT versus line voltage.

From the Eq. (5) and Eq. (6) it is clear that the diode D_1 and the diode D_2 do not conduct simultaneously. So, when D_1 will conduct D_2 will not conduct vice-versa. Thus there are two modes of operation. Figure 14 shows the operation modes of flyboost PFC cell.

Thus there are two modes of operation:

(1) Flyback Mode

(2) Boost Mode

Flyback Modes of Operation: it is easy to understand for the interval when line voltage $|V_{in}(t)|$ is less than $V_{cb} - n_1 V_o$ transformer T_1 work as a flyback transformer. It discharges all its energy directly to the load. Thus power transferred directly. This portion of power is processed by active switch only once. At the same time DC/DC cell will deliver some power from bus capacitors to the load to improve output voltage regulation. Operational waveform in this mode is shown in Figure 15. There are three interval of operation in flyback mode.

(1) First Interval: When switch is on at t_o rectified line voltage is applied to the transformer T_1. Transformer T_1 work as a flyback transformer. Power is transferred to the load at the time when switch is off. The bus capacitors voltage is applied to the inductor through the transformer T_2 for the regulation of output voltage. The special configuration of parallel-series forward conversion cell is useful for controlling DC bus voltage.

(2) Second Interval: When switch is turned off at t_1, energy is transferred by transformer T_1 to the load so voltage across T_1 will be $n_1 V_o$. Freewheeling path of diode D_6 is through output inductor L_o. Transformer T_2 resetting its energy through bus capacitors by the help of diodes D_2–D_4. Voltage across switch is clamped to sum of capacitors, C_1, C_2 voltage. Thus the switching voltage is reduced by this configuration.

(3) Third Interval: At t_2 all magnetizing energy of transformer T_1 is transferred to the load. Now the current of secondary winding of transformer will be zero. Transformer T_2 continues to reset through the bus capacitors, since it is fixed to bus voltage.

Boost mode of operation: When line voltage $|V_{\text{in}}(t)|$ is higher than $V_{cb} - n_1 V_o$ transformer T_1 works like a boost inductor. All magnetizing energy of both bus capacitors is discharged via D_2 and DC-DC cell delivers all output power from bus capacitors to the load. Thus power processing two times by the active switch. The operational waveform is shown in Figure 16. Circuit operation in this mode is same as flyback mode in the first and third interval. But for the second interval it is different. In the second interval primary current of

transformer T_1 will decrease. The current of output inductor freewheels through diode D_6. Transformer T_2 is resetting through diode D_3–D_4. The transformer action of flyback transformer is not working. This is due to reverse biased nature of flyback transformer diode D_1. Therefore output current of secondary transformer is zero in this mode.

6. Simulation Results

The circuit shown in Figure 13 has been simulated in Matlab, the simulation results is shown in Figures 17, 18 and 19. The operating switching frequency is 50 kHz. As Figure 17 shows the input current tracks the input voltage so input power factor is almost unity. The two modes of operation, flyback mode and boost mode are clearly specified in Figure 17. As shown in Figure 18, bus voltage is fixed at 420 V; so switching stress is not high. Output voltage is almost fixed at 30 V, so it is well regulated. Simulation is done for 100 W AC/DC converter.

The Figure 19 shows currents in different cells. As the requirement is PFC cell works on DCM mode and DC-DC cell works on CCM mode, it is clearly specified in Figure 19. Secondary winding current of flyback transformer carry current only in flyback mode, in boost mode primary winding of flyback transformer works as a boost inductor.

Figure 20 shows bus voltage versus line voltage at different turns ratio. As turns ratio of transformer T_1 increases bus voltage increases almost linearly.

Figure 21 shows DC bus voltage output inductance value of forward DC-DC cell. As output inductance increases DC bus voltage increases. Again it is a function of turn ratio of flyback transformer, higher the turn ratio lowers the flyback mode, lower the direct power transfer and so lower the efficiency. But small turns ratio will results in very low bus voltage, which may cause PFC cell to operate under CCM. Since there is no active control over PFC cell, it will cause very high peak current. So, it limits the minimum turns ratio value. Hence, in order to achieve lower bus voltage, L_1 should be as large as possible, while n_1 and L_o should be as small as possible.

Figures 22 and 23 shows the direct power transfer versus bus voltage and line voltage. Higher the line voltage and bus voltage higher will be the direct power transfer.

7. Conclusion

From above discussions in this paper, it is clear that the power factor correction is being given significant importance for low power applications. Also as power electronic equipments are increasingly being used, they pose a serious problem of low order harmonics on utility side. Among various schemes available for PFC, the single stage scheme is best suited for low power application because of its cost effectiveness. But in this scheme, there is a serious limitation of high dc link voltage rise under light load condition. This problem can be addressed by using the concept of Direct Power Transfer. From the simulation and experimental results of DPT topology, it is clear that DPT is an effective way to control high dc link voltage and hence reduces the component stresses. This topology also maintains a good source power factor and a tight output voltage regulation without compromising with high DC bus voltage. Moreover, the efficiency of overall power conversion is high.

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