Extraction of Chip Power Delivery Current and Activity Variations

I. Kantorovich, V. Drabkin, C. Houghton, and J. St. Laurent Intel Corporation, USA

Abstract—It is extremely difficult to directly measure power delivery current on chip under operating conditions. We discuss an approach of extracting PDS current through measurement of impedance of power delivery system and voltage. Because impedance extraction, in turn, requires knowledge of power delivery current, we use a controlled process for which power delivery current can be predicted. The paper provides a method of current extraction for impedance measurement.

1. Introduction

Current on power delivery system (PDS) of a chip and activity variation are major indicators of chip and package performance. Knowledge of PDS current is also important to assess worst case power delivery noise [1]. Current on a functioning die is generated by chip operation. Therefore it cannot be measured directly. The only exception is the case when chip activity is unchanged (for example, when the only process on chip is clock operation). In this case PDS current averaged over clk period is DC current which can be measured directly in any accessible location of power delivery loop far from chip. Because in general on-chip current is AC we need to look for indirect methods of current extraction. Because measurement of PDS voltage is easy to perform on a functioning chip, PDS current can be extracted from measured PDS voltage if PDS impedance of a chip is known [2]. There are two major obstacles preventing from measurement of PDS impedance on a functioning chip. First, because chip and package are not separated, a longer interconnect is required to allow connection with the probe. On-die PDS impedance is very low, in milliohm or sub-milliohm range, which is thousands time less than impedance of connecting wires. The second obstacle is that to extract impedance one needs to know both PDS voltage Vcc and current Icc, so we return to the problem of current extractions. In conventional methods involving VNA [3], current is injected into the system and can be measured directly. Although an attempt to extract PDS current on operating chip using PDS impedance stumbles, looping back to the problem of measurement of PDS current, it has an advantage: Instead of extracting PDS current for an arbitrary unpredictable computer process we can now focus on a particular controlled process of our choice because impedance of PDS does not depend on variations of chip activity.

The paper discusses an approach of extracting PDS current through measurement of PDS impedance and voltage. For impedance measurement we consider a controlled process for which PDS current can be predicted. The paper provides a method of PDS current extraction for impedance measurement and considers a methodology of extraction of PDS current and switching activity variations for any computer process.

2. Choice of Controlled Computer Process for Impedance Measurement

The controlled computer process must enable one to measure a magnitude of current, and since only direct on-die current can be measured the computer process has to contain long intervals with unchanged chip's activity. The computer process should also be simple because to extract impedance and current one needs to use Fourier transform and solve de-convolution problem which is sensitive to noise. Therefore the computer activity profile must be as simple as possible to avoid impedance to be dumped by noise. In [4-7] we suggested to use a computer process in which chip activity changes step-wise. The step-wise computer process is a good candidate to meet the above requirements. This process has a wider bandwidth than any continuous process. Several methods of generation of step-wise computer activity have been presented. For EV7 microprocessor measurements we used a specially designed computer code [4]. Advantage of this method is that it does not require any special hardware arrangements. We also used a method in which step-wise activity was generated by toggling clock frequency between two levels [5, 6]. In this method the profile of chip activity is far less noisy than the computer code method. A particular case of clock toggling is switching clock on and off [7, 8].

3. Extraction of PDS Current for Step-wise Computer Process

The rise/fall time limits the bandwidth of PDS current and impedance measurement. For activity step generated by toggling clock frequency the transition time is about one clock period. For step-wise process we need to make an assumption about current behavior in the vicinity of the transition period. In [4-6] it was assumed that current is unchanged beyond transition and changes linearly within the transition interval (trapezoidal current). This assumption was adopted in other applications of this approach. [7,8]. However, more detailed consideration of the current behavior shows that the mean PDS current (averaged over the clock period) is not trapezoidal. This can be derived from the correlation between the mean PDS current *Icc* and mean voltage on PDS Vcc of a chip:

$$Icc = C * F_{cl} * Vcc, \tag{1}$$

where F_{cl} is the clock frequency and C is the effective "switched" capacitance, which depends on the number of switching gates at a given state. According to Eq. (1), PDS current is not trapezoidal because voltage profile is not trapezoidal. From measurements it is known that voltage response to step-wise changing activity (step response) has a rippled profile after transition, exhibiting one or more droops. This means that, PDS current may not contain long unchanged intervals far from transitions, which are needed to provide us with reference points for current measurement. Therefore even for a simple, step-wise, change of chip activity PDS current has a complicated profile and there is no sections on current profile for which current can be measured directly. To resolve the problem, note that according to Eq. (1) chip can be formally characterized by an equivalent conductance G:

$$G = C * F_{cl}.$$
(2)

Because effective capacitance and/or clock frequency change when computer activity changes, for a computer process where chip activity toggles between high and low levels, the equivalent conductance will also toggle. We prefer to use conductance instead of resistance, because the transition time for conductance, unlike for resistance, properly represents the bandwidth of the process. We will use a representation of a chip through variable equivalent conductance to extract PDS current for the step-wise process. Figure 1 shows a simplified equivalent circuit for the power delivery loop.



Figure 1: Simplified equivalent circuit of power delivery system.

The right hand side shows a chip represented by variable equivalent conductance. On the left hand side is a PDS block, which includes power delivery network on PCB, package and die. It also includes a DC voltage source. For the right-hand side, we can represent current as

$$Icc = G * Vcc \tag{3}$$

which is Ohm's law in time domain. This equation allows one to determine PDS current for a step wise process if variable conductance is known. Fourier component of PDS impedance Z can be determined from the convolution equation valid for PDS block in Figure 1. It is presented in the form of Ohm's law in frequency domain:

$$Z = -Vcc(f)/Icc(f), \tag{4}$$

where f is noise frequency. Eq. (4) is not defined at zero frequency. Note that we independently use Ohm's law twice to determine both PDS current and impedance. In this solution the problem of extraction PDS current is reduced to the problem of extraction variable equivalent conductance of the chip for a step-wise computer process. Because equivalent conductance changes step-wise, we need to know its high and low levels. We measure them separately in two independent computer runs, in which the only process running on-chip is a process with unchanging activity on either high or low level which will be used later on in activity toggling. In each run we simultaneously measure the mean voltage between power and ground on chip and the mean current. We cannot measure current on-chip, so we measure it far from chip, on voltage regulator, because current is unchanged. Each conductance level is determined as a ratio of measured current and voltage.

It is important to accurately measure Vcc profile to avoid noise in impedance profile, because current for any computer process is determined using division by impedance. Most of the noise is a random noise which can be excluded by averaging over many Vcc waveforms. Regular noise can be identified by changing clock



Figure 2: Typical measured raw Vcc (black) and Vcc after noise is filtered out (white).

frequency or measurement setup [6]. Figure 2 shows a typical measured raw Vcc (black trace) and Vcc after noise is filtered out (white trace).

In the methodology we have just discussed we measure directly only PDS voltage on-die and current on voltage regulator. With these measurements no calibration and compensation of parasitics is required which is a nightmare for traditional methods of low impedance measurements using VNA or impedance analyzers. Note also that by solving the problem of *Icc* extraction, we actually eliminated the problem of very long interconnect in measurement of very low impedance.

4. Comparison of Different Methods of Icc Extraction for Step-wise Process

Consider differences between impedance determined through variable conductance representation of a chip, and assuming trapezoidal current. We do not expect difference in impedance resonance frequencies because in variable conductance case current ripples follow Vcc ripples, so resonance frequency is the same as for Vccresonances for both assumptions. However, resonance peaks may be different, because Icc varying in accord with voltage variations can make impedance resonances more pronounced than in the case of trapezoidal current. Figure 3(a) shows voltage and current waveforms in time domain for measurement simulation made for a Spice model of a future generation chip. One can see that Vcc has an overshoot, and it rapidly returns to its value before transition. This system has a high Q-factor. Figure 3(b) shows voltage and current in frequency domain. We can see that both voltage and current for "variable conductance" case have pronounced resonances. The trapezoidal current does not have resonances.



Figure 3: PDS current and voltage for measurement simulation in time (a) and frequency (b) domains.

Figure 4 shows impedance of this chip for the two cases. One can see that assuming trapezoidal current on-chip (white trace) we get to a significant, 3-fold, underestimation of the resonance impedance.

Consider measurement results for EV7 microprocessor. This system has a 3-fold higher decoupling capaci-



Figure 4: PDS impedance for measurement simulation.

tance and an order of magnitude higher resistance in the decoupling loop then in the previous case. Figure 5(a) shows that Vcc after the first droop restores slowly so that the noise at maximum is still half of the noise at the first droop minimum. The Q-factor for EV7 chip is lower than in the previous example. Figure 6 shows PDS impedance of the EV7 chip, extracted using the two assumptions on Icc. There is no significant difference between the results obtained using both methods. Figure 5(b) provides an explanation. It shows Fourier components of measured Vcc and the two currents. The voltage resonance at 60 MHz is shallow, so that the respective current resonance for "variable conductance" case is hardly noticeable on the steeply declined current profile. Figure 7 shows the relative difference between values of impedance determined by the two methods plotted versus Q-factor. The difference goes up linearly with the increase in Q-factor.



Figure 5: PDS current and voltage for EV7 chip in time (a) and frequency (b) domains.



Figure 6: PDS impedance for EV7 chip.



Figure 7: Relative difference in PDS impedance.

5. Extraction of PDS Current for any Computer Process

Once PDS impedance on chip is known one can extract PDS current for any computer process, not only step-wise process, by using a de-convolution procedure. Maximum ΔIcc can be obtained running extreme processes with maximum activity changes (power viruses). To extract the current signature we measure PDS voltage, and apply FFT to convert Vcc to frequency domain. Dividing voltage by known impedance we can obtain PDS current in frequency domain. Then we apply inverse Fourier transform in order to convert PDS current from frequency to time domain. Since PDS impedance is not defined at zero frequency, the de-convolved PDS current is determined up to an additive constant and a reference current is required to determine Icc. The way to obtain the reference current is to measure Icc at voltage regulator simultaneously with measurement of Vcc on-die. This current is averaged over time and is used as a reference for the averaged de-convolved PDS current. Figure 8 shows a fragment of measured Vcc on EV7 chip running the power virus SWIM, and Figure 9 shows the de-convolved PDS current on-chip.

6. Extraction of Activity Variations

We used a term "chip activity" to qualitatively characterize a computer process. Equivalent conductance can serve as a quantification of the chip's activity. It best represents the chip activity because supply current is consumed through switching of on-chip capacitive loads. Changes in activity result from changes in the magnitude of the capacitive loads or from changes in the frequency at which the capacitive loads are switched. Because equivalent conductance variation depends on the same changes, the variance in switched activity is equivalent to a variance in chip equivalent conductance. Actually, chip's activity rather than chip's PDS current can be considered as a stimulus producing PDS noise. The chip's current is less appropriate because it is affected by the *Vcc*. Therefore, for PDS noise characterization we need to know ΔG rather than ΔIcc . We can determine variations of the chip's activity or equivalent conductance dividing measured PDS current by voltage in time domain. Equivalent conductance variation for EV7 chip is shown in Figure 10. From Figure 10 one can extract maximum ΔG , knowledge of which is necessary to obtain the absolute maximum PDS noise for a chip.



Figure 8: *Vcc* on EV7 chip running power virus SWIM.



Figure 9: Icc on EV7 chip running code SWIM.



Figure 10: Equivalent conductance variation on EV7 chip running power virus SWIM.

7. Conclusion

There are no direct methods of measurement of PDS current on functioning die. Current can be extracted indirectly from measured *Vcc* if PDS impedance is known. Measurements of PDS impedance, in turn, requires

knowledge of PDS current. The solution we suggested is to generate a step-wise computer process and predict PDS current for this process using equivalent conductance representation of a chip. Equivalent conductance can serve as a quantification of chip switching activity. PDS current and chip activity for any computer process can be determined by de-convolution involving measured Vcc and known PDS impedance. The measurement are easy to perform because only Vcc on-die and current on voltage regulator are measured directly so we can avoid calibration and compensation that are most challenging parts for conventional measurement techniques. The proposed methodology is the only available methodology for measurement PDS current and activity variations on a functioning chip

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