Noise Source Characterization on the PDN for EMI

M. Lai[1], **V. Ricchiuti**[2], **A. Orlandi**[3], **B. Archambeault**[4], **G. Antonini**[3]
D. J. Pommerenke[1], **and J. L. Drewniak**[1]

[1]University of Missouri Rolla, USA
[2]Siemens C.N.X., Italy
[3]University of L'Aquila, Italy
[4]IBM, USA

Noise resulting from IC activity is easily distributed throughout an electronic design as a consequence of a low-impedance power distribution network in a multi-layer printed circuit board. Both EMI and SI problems can result as a consequence. The passive portions of the PDN are being successfully modeled with full-wave formulations, as well as circuit extraction approaches, which provide design insight and methodologies for the PDN. However, in order to determine specific total capacitance needed, as well as quantify the voltage on the PDN, a suitable noise source model is needed for the ICs. This work details a frequency-domain approach for extracting current noise source models from swept-frequency methods.

The core and I/O activities in a common IC have different contributions to the global noise level in the full system. In order to better understand and quantify the specific weight of each, a methodology for estimating these two distinct but simultaneous noise sources is being developed. The estimation of the noise current by means of S-parameters and power spectra measurements is proposed here for a 208 pin, 155.52 MHz clock FPGA characterized by two voltage logic levels, 1.8 V for the core and 3.3 V for the I/O. From the measurement of the power spectra at the two logic levels in a position that can be considered coincident with the FPGA itself and from 2-port S-parameters measurement, it is possible to model the noise currents sources associated with the core and I/O respectively. The method is validated by estimating the same noise current sources also from a remote location from the FPGA itself, and it is done by adequately taking into account the effect of the transfer impedance between the ports and the FPGA. The effect of the SMA connectors used to perform the measurement is removed by means of a de-embedding procedure. The noise current sources are fully characterized in terms of magnitude and phase by means of a Hilbert transform procedure using the measured power spectra. In order to take in account only the effect of the activity of the FPGA, the power spectra are filtered from the effect of the external clock. The obtained noise current sources can also be characterized in terms of different load conditions by changing the number of I/O outputs simultaneously switching, allowing the estimation of an upper and lower limit for the sources.