

VEMC Computing System for Electromagnetic Compatibility of Integrated Circuits

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Abstract— This paper introduces a newly developed virtual electromagnetic compatibility (VEMC) computing system and related techniques for electromagnetic compatibility (EMC) computer modelling, simulation and optimisation in integrated circuit (IC). The system is a high performance computation and collaborative visualisation platform which provides researchers and engineers with an integrated and flexible computation environment in modeling, simulation and optimisation of IC EMC issues. It meets various computation needs and increases machine usage and computation efficiency of computation resources. A case study presents computational models of interested issues in IC-level EMC modelled, simulated and optimised by the developed system.

1. INTRODUCTION

In modern IC-level EMC, computational electromagnetic (CEM) modelling and visualisation techniques become most significant considerations [1–3]. They are now an integral part of design in engineering practice and implemented to solve real life EMC problems which is proved extremely important for this high EMC risks industry. Traditional “build then test” procedure for EMC was proved time consumed and very expensive in terms of cost. CEM modelling and visualisation allows designer to investigate, monitor and modify the interested area of the design at an early stage, which makes it play an important role in scientific research and industry applications of IC.

Visualisation and high performance computation are closely related that utilizes visualisation techniques to deal with the complicated dynamic electromagnetic problems. Due to the variety and complexity of different IC EMC problems, it always requires engineers from different disciplines work collaboratively to analyse and optimise the solution together. Using interactive and collaborative visualisation techniques [4] provide an alternative solution to achieve best performance and efficiency of teamwork. However, current CEM products and systems are still dominated by single user oriented designs.

The virtual electromagnetic compatibility (VEMC) computing system is a high performance distributed and parallel computation and visualisation system designed for requirements of high-load EMC modelling, simulation and optimisation tasks. Parallel and distributed computation is supported. It integrates a full electromagnetic modelling and simulation environment with various pre-defined model libraries and templates. The system uses cloud computing concept to offer users a remote working environment on the modelling and simulation. With this system, users do not need to install huge amount of professional software. The cost of entire system is well controlled comparing to professional supercomputing cluster structure due to its generic business computer based.

2. VEMC COMPUTING SYSTEM

2.1. System Architecture

The VEMC computing system uses a distributed computing architecture. It is a structure that involves multi-computers collaborating remotely from each other. Every computer under this architecture will be assigned a role in the computation or data processing. As shown in Figure 1, the cloud controller (CLC) is the main server of system which is used to provide multi-functions of access authority, load balance, license management, gate way and firewall. The user information and database are stored in the database (DB). A web service manager (WSM) is connected with CLC to provide system GUI. The cloud storage pool (SP) contains a pre-defined model library, virtual machine OS image file and other software image. Computation nodes are scalable in the system according to user’s demand.

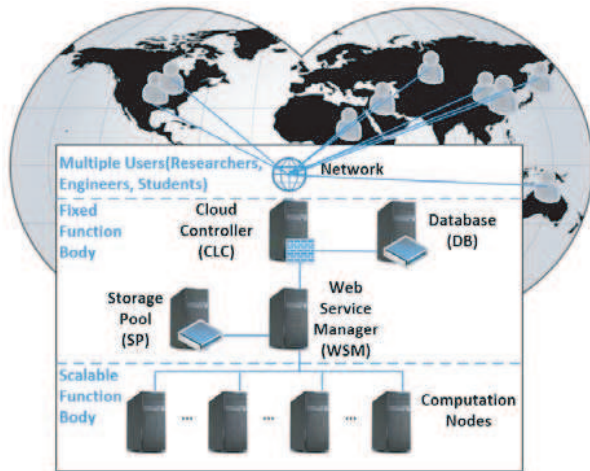


Figure 1: VEMC computing system structure.

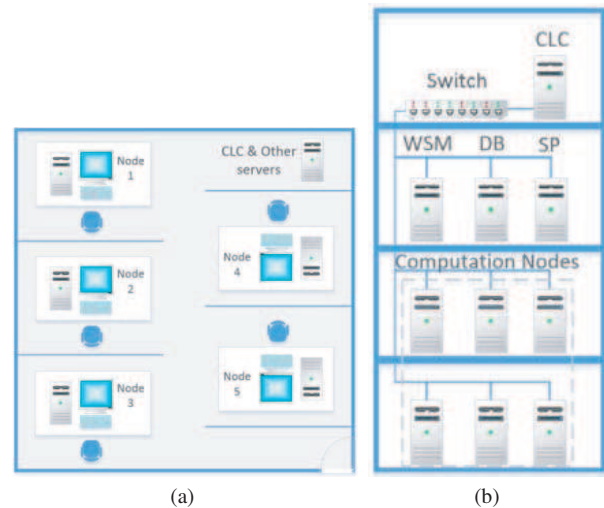


Figure 2: (a) Distributed structure and (b) assembly structure of VEMC computing system structure.

2.2. System Features

2.2.1. Cost Effective and Scalability

The VEMC computing system is built up with generic desktops which is found much cost effective and flexible. Computation using supercomputer can provide user with extreme performance but the system itself is high cost, hard to maintain and has an unfriendly interface. As compared in [5], it is surprised to find that the generic business desktop has the lowest cost per megaflop/s comparing to other supercomputing platforms. The cost of system is directly against the number of physical machines.

The architecture of VEMC computing system is very flexible, as shown in Figure 2. It can be setup and implemented according to the teaching demand. For any organizations, even old computers can also be assigned as computing nodes and added into the system. All computer nodes in the system are able to be added and removed as required, which means the system is of a strong scalability to satisfy the demand of students scale. It is also power efficient as the administrator can decide how many nodes to be turned on and off at any time.

2.2.2. Cloud Computation and Advanced Control

As a cloud computing based computation system, it enables a convenient, on-demand network access to a shared pool of configurable computing resources [6]. The user just needs to connect with the cloud and then can work anywhere anytime. The computer hardware resources, such as CPU core number, memory size, and disk space can be allocated within seconds by the request of end-user. The user can setup a new working environment by importing the pre-configured image file from the cloud storage system server in a few minutes.

VEMC computing system automatically controls and optimises resource by a newly developed load balance control system. Resource usage can be monitored, controlled and reported by both service provider and user. Also, the system supports real-time process migration that secures user process and avoids data loss from system corruption.

2.2.3. Collaborative Visualisation

The system allows multiple users to access same project simultaneously under a secured channel across different platforms using collaborative visualisation techniques, as shown in Figure 3. Thus, it offers great convenience for multiple users, for example, a group of students, to discuss and collaborate on one modelling or simulation project. The template is used to format your paper and style the text. All margins, column widths, line spaces, and text fonts are prescribed; please do not alter them. You may note peculiarities. For example, the head margin in this template measures proportionately more than is customary. This measurement and others are deliberate, using specifications that anticipate your paper as one part of the entire proceedings, and not as an independent document. Please do not revise any of the current designations.



Figure 3: Collaborative visualisation across different platforms.

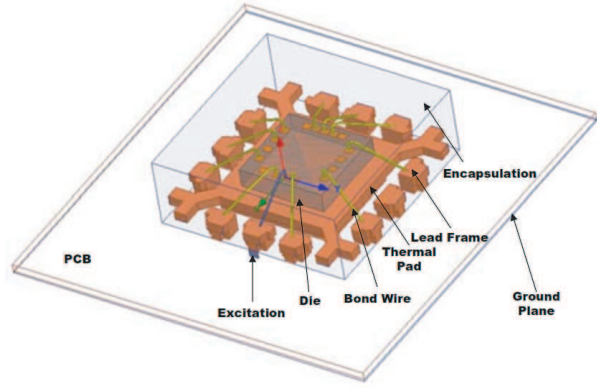


Figure 4: Simulation model of MMIC.

3. COLLABORATIVE SIMULATION OF A MONOLITHIC MICROWAVE INTEGRATED CIRCUIT (MMIC)

EMC of IC cannot be neglected in the modern electronic system due to the constant speed of growth in semiconductor technology. Therefore, IC-level EMC has taken an important position in the modern IC design. Comparing to traditional procedure of IC design, it requires more collaborative work when considering IC-level EMC. There is one prototype VEMC computing system available at Nathan campus, Griffith University, which conducts following modelling, simulation and optimisation in IC EMC.

3.1. MMIC Simulation Model

The MMIC operates at 24GHz in a small and high frequency device. The chip is packaged in a quad-flat no-leads (QFN) package with 12 pins. The size of the QFN package of the MMIC is 2 mm (length) $\times$ 2 mm (width) $\times$ 0.75 mm (height). The QFN package technology mounts the IC directly onto the surface of the PCB with no through-holes. The internal connections between the die and lead frame are bond wires. The simulation model is as shown in Figure 4. The excitation is set up at a lead, which is functioning as the only microwave port in the physical model. Some critical size parameters of the model are shown in Figure 5.

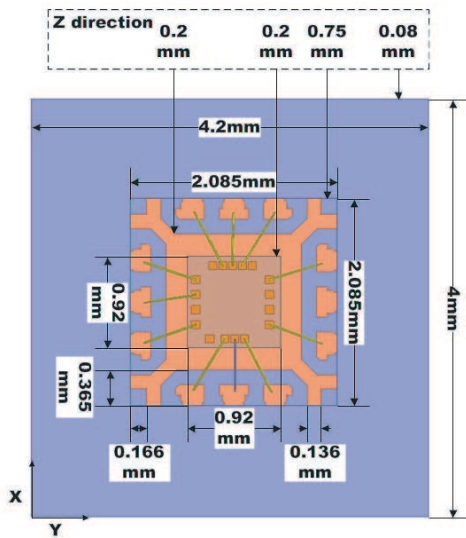


Figure 5: Size of simulation model of MMIC.

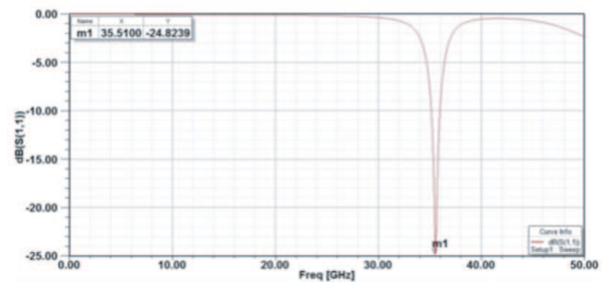


Figure 6: Reflection coefficient of the simulation model from 0 to 50 GHz.

The radiation boundary condition is used as a box shape surrounding the model. The materials assignment of the simulation model is described in Table 1.

Table 1: Materials assignment of the simulation model.

Name	Materials	Permittivity	Conductivity (Siemens/m)
Ground Plane	Copper	1	5.8×10^7
PCB	FR4 epoxy	4.4	0
Die	GaAs	12.9	0
Encapsulation	EME-G770HCD	4.2	0
Thermal Pad	Copper	1	5.8×10^7
Lead Frame	Copper	1	5.8×10^7
Bond Wire	Copper	1	5.8×10^7

3.2. Full-wave Techniques in the Frequency Domain

A full-wave electromagnetic solution, which solves electromagnetic problems with Maxwell's equations, is of great importance to high performance VLSI design in computational electromagnetics. With numerous fast numerical algorithms developed, the finite element method (FEM) is relatively efficient in finding approximate solutions of partial differential equations (PDE). The frequency domain vector wave equation for E field can be derived as:

$$\nabla \times \frac{1}{\mu} \nabla \times \vec{E} + \sigma_e \omega \vec{E} + \omega^2 \epsilon \vec{E} = -j\omega \vec{J} \quad (1)$$

where ω is the angular frequency, J is the source current density, σ_e is the effective conductivity, and μ and ϵ are the permeability and permittivity of the problem space respectively.

Simulations in the followed discussion are applied by a full-wave frequency domain solution with variable sized meshes. Frequency is set up to sweep in a specific range to determine the expectant resonant frequency. However, determining the correct frequency range is important for simulation results. Computational errors may be introduced if the frequency range of the solution is mismatched.

3.3. Simulation Results

Simulation is conducted under an excitation with the frequency swept from 0 to 50 GHz. The reflection coefficient plot shows there is a resonant frequency occurring at 35.51 GHz with -24.8239 dB as shown in Figure 6.

An E field plot of die surface at 36.01 GHz is produced in Figure 7. It is found that the electric field intensity is highest in the centre position at 1.5998×10^3 V/m.

As presented in Figure 8, the simulation result shows radiation power emitted vertically along the $+Z$ axis. The power radiating underneath the model is very weak.

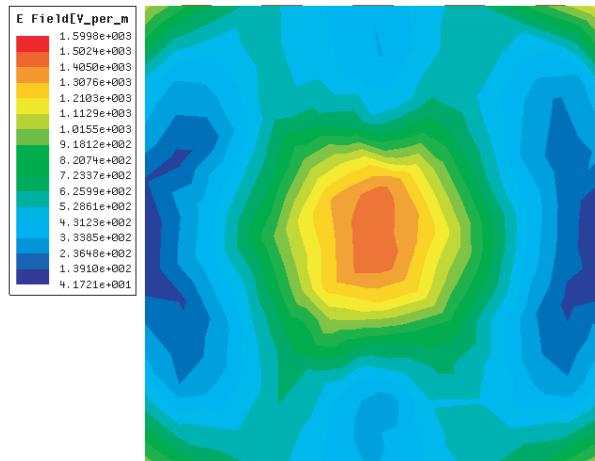
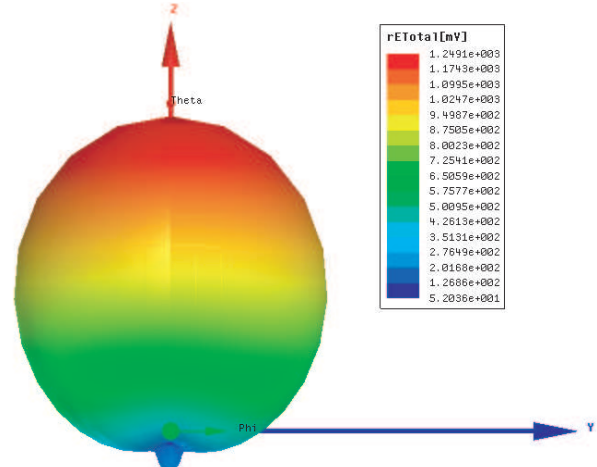
Figure 7: E field simulation plot of die surface.

Figure 8: Far-field 3-D plot of the simulation model at 36.01 GHz.

4. PARALLEL OPTIMISATION OF MULTI-LAYER INTERCONNECTS

Parallel computation is another key attribution needed for IC EMC, especially in optimisation. For instance, optimisation of coupling issue regarding to multi-layer interconnects of IC requires a high load of computation resource.

4.1. Structure Modelling for MultilayerInterconnects of IC

As shown in Figure 9, it is an advanced multilayer structure for interconnects of IC. There are five levels of conductors inside two isolated layers upon a silicon substrate. Each layer is isolated by a low permittivity material. The population $G(t)$ for optimisation is the matrix of $[X1, X2, \dots, X8, Y9, Y10]$, as shown in Figure 10. With different combination of conductor positions, it varies the total ground capacitance and the total coupling capacitance of interconnects. The aim of this optimisation is to find out the best allocation of conductors which contributes to the lowest value for the trade- off between total ground capacitance and total coupling capacitance of interconnects.

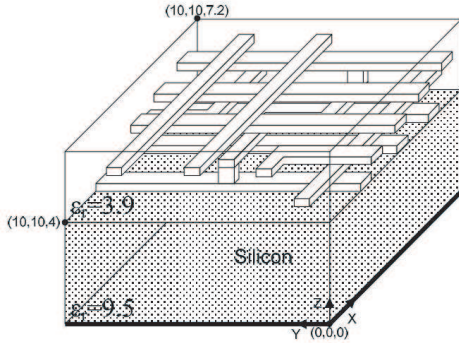


Figure 9: 3D multi-layer interconnects for optimization.

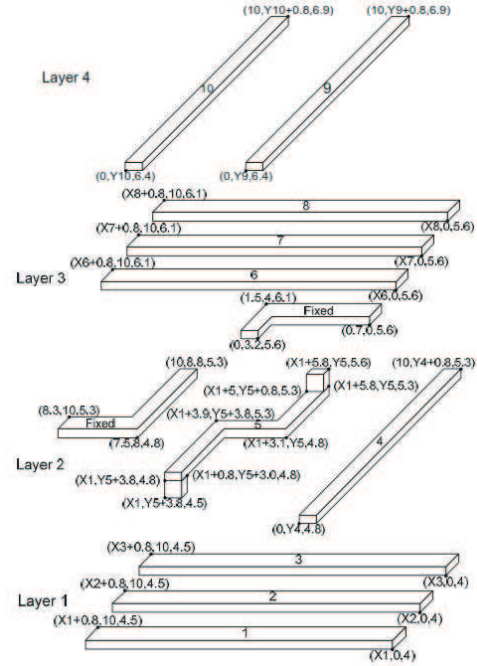


Figure 10: Dimension details of 3D multi-layer interconnects.

4.2. Capacitance Calculation Methodology

An accurate and fast method of capacitance calculation is to apply the principle of energy conservation using electrical field energy stored in the volume V . The electrostatic energy of a linear N electrode (the N th is ground) system is:

$$W = \frac{1}{2} \sum_{i=1}^N C_{ii}^g V_i^2 + \frac{1}{2} \sum_{i=1, j=1, i \neq j}^N C_{ij}^g V_i V_j \quad (2)$$

where, W is electrostatic energy; V_i or V_j is the potential of i th electrode with respect to the ground; C_{ii}^g is the self-ground capacitance of i th electrode and C_{ij}^g ($i \neq j$) is the mutual ground capacitance between electrodes. By applying appropriate voltages on electrodes, the coefficients of the ground capacitance can be calculated from the stored static energy.

4.3. Optimisation Method Applied via VEMC System

The selected optimisation method is the improved version of non-dominated sorting genetic algorithm (NSGA), NSGA-II [7]. It performs a fast multi-objective evolution in terms of finding a diverse set of solutions and in converging near the true Pareto-optimal set. The first step initialized the population (size N) based on the defined problem range and constraints. Then the non-dominated sorting is applied on initialized population, which is sorted based on non-domination

into each front. The first front is completely non-dominant set in the current population and the second front is dominated by the individuals in the first front only, and the front goes so on. After non-dominated sorting is done, the crowding distance is calculated and assigned for all individuals in the population. Based on the rank and crowding distance, parents are selected for evaluation manipulation which generates the offspring population. The current population and generated offspring will be combined again based on the non-domination. Only the best N individuals are selected for new population and others are truncated. Thus, iterations continue until stop criterion is achieved.

With Matlab and Java script, the parallelism used the structure as shown in Figure 11. The master node executes NSGA-II code and assigns parallel tasks to slave nodes. The slave nodes perform FEM simulation and calculate capacitances of assigned structure. The results will be collected by master node and process repeats. The entire procedure of optimisation involves 100 groups of generation.

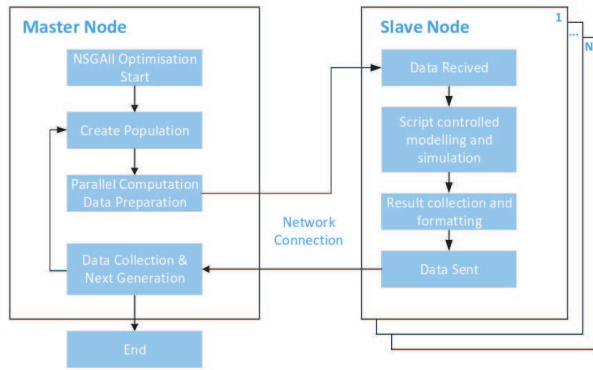


Figure 11: Parallel computing for NSGA-II.

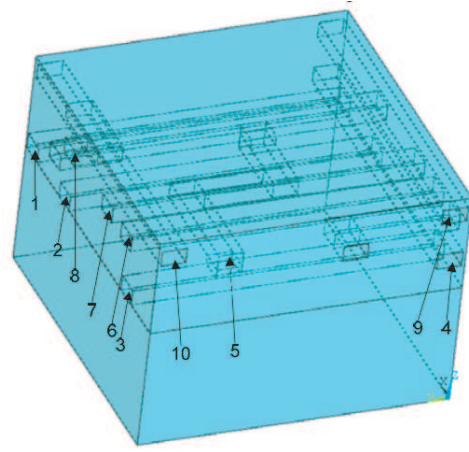


Figure 12: Optimized Structure of 3D multi-layer interconnects.

4.4. Optimisation Result

One of final optimized 3D structure is plotted in Figure 12. According to the figure, all parallel interconnects are separated widely to avoid coupling capacitance between each other. In addition, the structural width of interconnects 9 and 10 minimized overlapping coupling capacitance compared with interconnect 5 and two other fixed “L” shape interconnects.

When optimisation is implemented in one single physical machine, the maximum CPU usage is only 20% and maximum memory usage is 63.7%. The total runtime of entire procedure is 52.60 hours. In VEMC computing system, computer resources can be used more efficiently under the support of virtualisation technology. When then optimisation is paralleled in three virtual computing nodes, the maximum CPU usage and maximum memory usage are increased up to 100% while the total runtime is significantly reduced to 19.32 hours which is roughly 1/3 of runtime in one single physical machine.

5. CONCLUSIONS

This paper introduced a VEMC computing system which was designed and developed with high performance computation and collaboration visualisation capabilities in order to fulfil the requirement of IC EMC in modelling, simulation and optimisation. In addition, the system can be easily applied with existing computer hardware in any computer facilities which greatly increases machine usage and efficiency while relief provider from the financial pressure of setting up a supercomputing environment. Collaborative simulation and parallel optimisation played critical roles in IC EMC. Two case studies demonstrated the performance of VEMC computing system applied in IC-level EMC. Case one demonstrated a collaboration simulation of a MMIC. Case two analysed the performance of VEMC computing system in a parallel optimisation of multi-layer interconnects of IC.

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