A 4 MHz-10-GHz, 10-ps/dec Dynamic Comparator Using Negative Resistance Combined with CMOS Input Pair

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Abstract— A high speed, low delay/log (ΔVin) dynamic comparator using negative resistance combined with CMOS input differential pair is proposed and designed in IBM 180 nm CMOS process technology.

1. INTRODUCTION

Comparators are very used in the Control loop of the DC-DC Switching Converters. In the loop of DC-DC Switching Converters, PWM generators uses comparator that compare Triangular wave with the difference DC-DC output voltage and reference voltage. Due to limited accuracy, comparison speed and power consumption, comparison of the input data is regarded as one of the limiting factor of the high speed VLSI data conversion system. There is a growing need for the development of low power, low voltage and high speed circuit techniques and system building blocks because of increasing demand for portable and hand held high speed devices. On the one hand, low voltage operation is required to use as few batteries as possible for low weight and small size. On the other hand at the high frequency of operation, Low power consumption is demanded to prolong battery lifetime as much as possible [1, 2]. In the recent decade, due to the rapid advancement in Analog-to-Digital conversion devices, the rapid advancement of VLSI technology causes the evolution of digital integrated circuit technologies for signal processing systems that operate on a wide variety of continuous-time signals including DC-DC switching converters, speech, medical imaging, sonar, radar, consumer electronics and telecommunications.

Already with voltage scaling, sub-threshold voltage region demands require technology for new architecture and innovative circuits. Previous advances in MOS technologies meet it for higher speed applications, however due to MOS device mismatches, it is difficult to achieve a high speed and accuracy at the same time [3].

One of the key components in PWM generators as the fundamental block for the A/D conversion, are the comparators. In fact they are the link between analog domain and digital domain for compare a set of variable or unknown values against that of a constant or known reference value [4]. Many DC-DC switching converters in the control loop demands high-speed, low-power comparators with small chip area. For low-voltage operation, developing new circuit structures is preferable in order to avoid stacking too many transistors between the supply rails [5].

The organization of this paper is as follows. Section 2 described the proposed dynamic comparator. Section 3 illustrates the simulation results. A comparison to the conventional comparators is also presented, followed by the conclusions in Section 4.

2. PROPOSED DYNAMIC COMPARATOR

2.1. Structure

The comparators are consists of two parts namely pre-amplifier and latch that these parts operate in the same phase. Therefore, comparator can pull the latch. In the second phase, the pre-amplifier output nodes up to the power supply voltage level. Also, the comparator offset can be cancelled in this phase [6, 7]. Consequently, the comparator offset effect has not been considered in this paper. Fig. 1 shows the circuit diagram has been used in simulations that has been obtained from [8] with adding Q2 and Q4 that a dual rail pre-amplifier is achieved. For decreasing the loading effect on the comparator output, two CMOS inverters have been used to supply capacitive loads. The comparator consumes dynamic power because the comparator consists of dynamic latch and pre-amplifier [9].

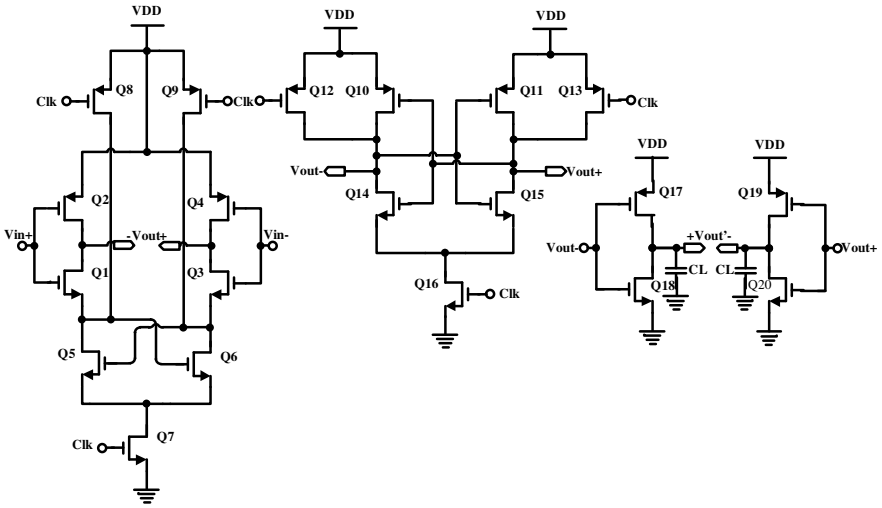

Figure 1: Schematics of the dynamic comparator and CMOS inverters.

2.2. Transient Behavior

Figure 2 shows the sketch map of the transient behavior of the dynamic comparator in the comparison phase. By the switching transistors Q8, Q9, Q12, and Q13 during the reset phase, the output terminals and the drain side voltages of Q5 and Q6 are all pulled high to VDD, respectively. By turning on the two tail transistors Q7 and Q16, the comparison phase begins. Therefore, the CMOS input stage transfers the differential small signal to the cross coupled stage. Q2, Q4 are activating when the input common mode is lower than the Q1 or Q3 threshold voltage. Therefore, the dual-rail differential input obtain since they are supplies the preamplifier output. Based on [10], the comparison transition can be divided into three phases (from phase 1 to phase 3). The output terminals are pulled down by two tail transistors Q7 and Q16 during the phase 1. Until one of the two output terminal voltages decreases to (V_{DD}–V_{thp}), the p-channel transistors Q10 and Q11 remain cut-off. The Q2 and Q4 activate when the cross-coupled stage composed from Q1, Q3, Q5 and Q6 cannot start. Therefore, the speed of proposed idea is more than paper [8]. In order to enhance the voltage difference between the output terminals, the cross-coupled inverters provide strong positive feedback in the phase 2. The transition state changes from phase 2 into phase 3 when one of the transistors Q14 and Q15 is cut-off. There is no static power dissipation since the current flows through these n-channel MOSFETs stop automatically after the transition. Fig. 3 shows transient behavior of the proposed dynamic comparator at 1 GHz. As seen, both of the output terminals are pulled low in the beginning of the compare operation. One of the output terminals charge through the p-channel transistor when the transition goes from phase 1 into phase 2.

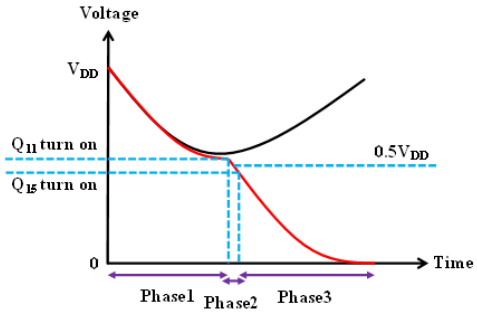

Figure 2: The sketch map for the transition behavior of the dynamic comparator.

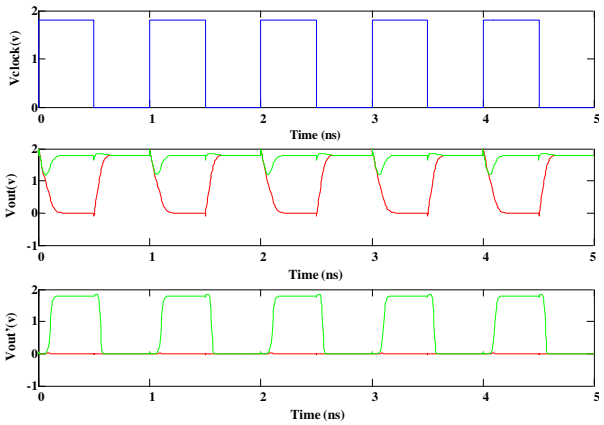

Figure 3: Simulated transient behavior of the proposed comparator structure.

Therefore, the strong positive feedback provided by these two cross-coupled inverters separates the output voltages. Against paper [8], this design aren't use from p-wells, thus the cost of comparator chip is lower.

3. SIMULATION RESULTS

In this paper for increase the simulation reliability, the post-layout simulation is done. The layout of proposed comparator shown in Fig. 4.

According to Fig. 4, layout size of proposed comparator is equal to 31.3 µm∗18.5 µm. For increase of the comparator sampling frequency to 10 GHz, the transistor layout designed based on multi-finger transistors. With this technique, the nodes capacitance of transistors is minimum; therefore the sampling frequency was minimized and the layout size was maximized. The av_extracted view of proposed comparator shown in Fig. 5.

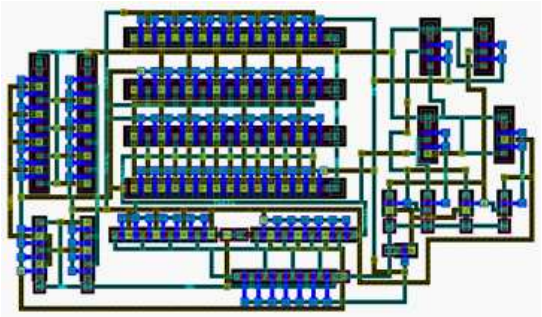

Figure 4: Layouts of the dynamic comparator and CMOS inverters.

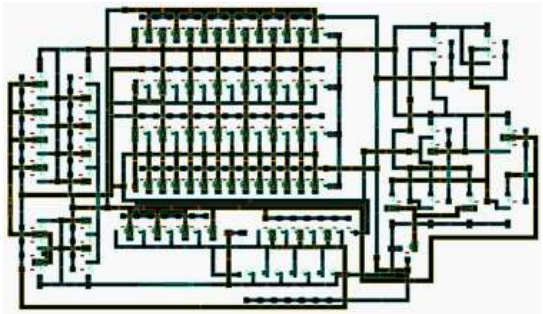

Figure 5: Av_extracted view of the dynamic comparator and CMOS inverters.

The Proposed idea simulated at the 180 nm CMOS model. The post-layout simulation results versus Sampling Frequency presented at the Table 1.

Table 1: Post-layout simulation results of the proposed comparator versus sampling frequency.

Sampling Frequency (GHz)	**0.004**	**0.01**	**0.1**	**1**	**5**	**10**
Resolution (mv)*	27	24	25	27	700	700
Power Supply (v)**	0.4	0.45	0.55	0.8	1.05	1.8
Power Consumption (µw)***	0.835	2.07	20.7	204.6	795.6	964

*Resolution calculated at 1.8 V DC power supply.

**Power supply calculated for maximum resolution.

***Power consumption calculated at maximum resolution and 1.8 V DC power supply.

For playing features of the proposed paper, we simulating the circuits at 180 nm CMOS that is a lower technology than recent reported papers but in this paper, the sampling frequency received to 10 GHz. The comparison State-of-the-Art Works between the proposed paper results and some other papers presented at the Table 2.

Table 2: Comparison to State-of-the-Art works.

Specifications	**[8]**	**[10]**	**[11]**	**[12]**	**This Work**
CMOS Process (nm)	90	Scaled to 90	90	65	**180**
Sampling Rate (GHz)	3	3	3	7	**10**
Supply/ICMV	1.2/1	1.2/1	1.2/1	1.2/1	**1.8/0.9**
Energy/decision (fJ)	71	88	90	185	**50.6**

The energy/decision for the proposed comparator is equal to 50.6 fJ that is highest value between papers at Table 2.

4. CONCLUSION

The proposed dynamic comparator structure has an added degree of freedom that enables higher input transconductance stage using negative resistance technique to get better delay/log (ΔVin) performance at low power consumption. Moreover, the structure is very suitable for advanced deep sub-micron CMOS process with lower threshold voltage to achieve higher operation speed for multi-giga Hz optical and data conversion systems. In this paper, we received to Energy/decision equal 50.6fJ at 10GHz.

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