A V-band Balanced MMIC Power Amplifier

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Abstract— A highly stable V-band balanced power amplifier has been proposed based on MMIC using the pseudomorphic High Electron Mobility Transistor (pHEMT). The amplifier consists of two stages with device length of $8 \times 25\,\mu m$ and $2 \times 25\,\mu m$ gate widths. The design kit of PP10 WIN Semiconductor Corp. has been used. The simulation results show power and gain levels of 18 dBm and 12.5 dB, respectively, with a tolerance of ± 0.8 dB over the broadband range of 40–80 GHz. Microstrip Lange couplers are used as 3 dB quadrature power splitters and combiners. The amplifier has an acceptable performance with low input and output VSWRs, high stability, fairly flat gain and constant power over the whole bandwidth; and so it can be a good candidate for broadband millimetre-wave front end transceivers systems, and also, as an instrumentation amplifier in measurement systems.

1. INTRODUCTION

Monolithic microwave integrated circuit (MMIC) is capable of giving uniform performance over a wide bandwidth in millimetre-wave frequencies, with small profile and less parasitic effects as well as cost-effectiveness in large-scale fabrications. As such, pHEMTs and mHEMTs are increasingly being produced on GaAs, GaN and InP substrates for improved performances for different applications in RF front-end, radars, sensitive military equipment and so on.

This paper presents an MMIC power amplifier that is capable of performing in backhaul communication of the next generation mobile networks. It can also be used as an instrumentation amplifier in measurement systems such as network analysers. It incorporates a balanced configuration (a widely accepted scheme for power amplifiers) with the use of hybrid couplers as power splitter and combiner. The balanced configuration compensates for the inherent drawbacks of power amplifier design and keeps this device stable whilst providing higher gain than a single-ended amplifier design using same technology [1].

2. DESIGN CONSIDERATIONS

2.1. Specifications

The amplifier is designed based on pHEMT technology and GaAs as substrate. The gate length of this device is 0.1 μm (formed using electron beam lithography) [2]. The substrate thickness is 50 μm that has better thermal properties and electron confinement than 100 μm substrat [3]. The amplifier is simulated on Process Design Kit (PDK) provided by WIN Semiconductor corp. From gain and stability analysis in [3] (110 GHz S-parameter measurement), the amplifier was found to provide a gain of 8–9 dB in the range of 70–90 GHz. According to [4], a typical GaAs pHEMT is capable of providing power density around 0.8 W/mm at 40 GHz and power-added efficiency (PAE) of about 10–30%, both of which decrease with frequency increase.

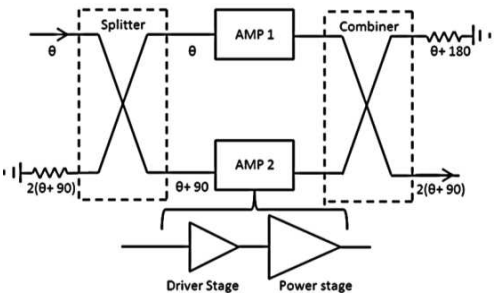

Figure 1: Balanced amplifier configuration.

2.2. Design Configuration

Following a balanced scheme, two identical power amplifiers are fed with 90° out of phase signals through a power splitter, shown in Figure 1. The amplified signals are then combined in-phase by means of a coupler placed (in reverse fashion) on the output of the amplifiers. This setup enables a higher gain though possibly at the cost of higher return losses. However, any reflected power is diverted to the matched isolated port of the coupler.

The interface impedance between individual amplifier and the quadrature coupler will remain standard 50 Ohm. Adopting the balanced configuration also means that an increase of 3 dB will be observed in the 1 dB compression point, $P_{1\,\mathrm{dB}}$ [5], while other characteristics of the amplifier stay the same. This increase is seen at the output port of the amplifier where coupler adds up signals from both branches and power gain of +3 dB is obtained. Similarly third order intercept point (3IP) increases by 9 dB and the stability is enhanced which gives design liberty. However, this is achieved at the cost of higher noise figure coming from characteristic noises of individual branches, dropping the overall SNR. Coupler insertion and signal losses are introduced by the use of microstrip coupler but not to a significant level. The quantitative observations are presented in next sections.

3. POWER AMPLIFIER DESIGN

Power amplifier (PA) has to be fed with a high amplitude signal so that the amplifier can operate at its compression point delivering maximum voltage and current. This is the point where PAE reaches its maximum value. Being at millimetre-wave frequencies, class E and F amplifier topologies have not been used since behaviour of the higher order harmonics, associated to substrate modes and possible radiations, are unknown. Instead, the PA is designed to be a two-stage Class A small signal amplifier with (1) Driver stage, (2) Power enhancing stage. The driver stage is designed to put the second stage into gain compression point while achieving high trans-conductance gain itself. The second stage is designed to deliver the highest possible power drawn from the pHEMT device. The output reflection coefficient (S_{22}) of power devices varies as a function of output power. The appropriate output matching network is also designed for the second stage ('power-match' rather than 'conjugate match') to provide optimum load impedance, hence maximising the output power, as calculated by Load pull analysis [6].

In order to get less parasitic effects in the driver stage, a small pHEMT device (with two-gate fingers) is chosen. The second stage uses eight-gate fingers. The gate width for each finger is 25 µm, which was initially estimated by observing power levels of [7]. This is thought to be optimal size as smaller device gives higher gain and large number of gate fingers characterise increased gate periphery, delivering more current and hence higher power.

3.1. Biasing and Stability

Forced stability was introduced in design of the biasing network for liberty in design at later stages. The stability factor was kept at the margin owing to the fact that balanced configuration, raises stability factor, k.

Figure 2 shows the I-V curves where all possible biasing points are plotted for different Gate-source voltages. The biasing point chosen was in the centre, located very close to m1 marker with VDS =2.5 V and VGS = 0.4 V. These values will run the amplifier as Class A.

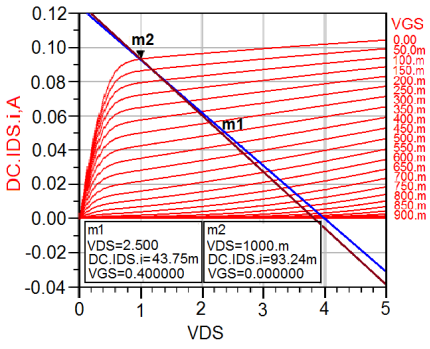

Figure 2: DC biasing I-V curves of the pHEMT.

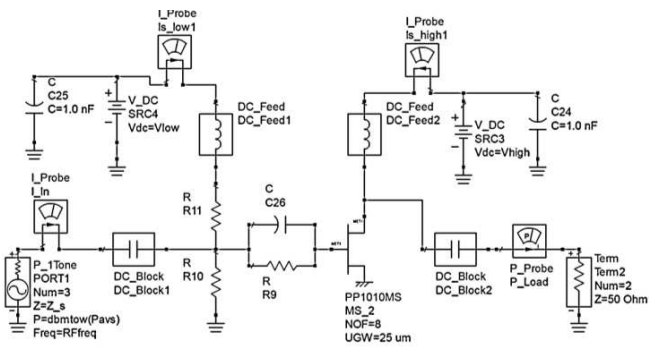

Figure 3: Schematic of the stable biased driver stage.

Introducing a small resistor (R9 in Figure 3) in series with gate feed line (shunt branch of R9 and C26) increases the stability factor. This will be at the cost of higher noise figure and maximum attainable gain of the device. In addition, connecting a shunt resistor to the drain compromises the maximum attainable power output. It was also found that changes on the input are more influential than at the drain. Inductors were used as bias chokes and DC blocking capacitors were utilised for isolation at input and output. Moreover, decoupling capacitors were added to avoid RF leakage. The operating point of both stages of the class-A power amplifier is chosen according to Figure 2.

The maximum voltage permissible in an energised GaAs pHEMT transistor is around 4 V. Using that convention, the biasing point chosen has drain-to-source voltage of 2.5 V and gate-to-source voltage of −0.4 V. The schematic diagram of the biased network is shown in Figure 3. Proper tuning of all components offers unconditional stability from 0 to 80 GHz.

3.2. Loadpull Analysis

The output matching network of power stage was formed through Loadpull analysis. The resulting contours of impedances obtained by Agilent Advanced Design Systems (ADS) software are shown in Figure 4, where all the impedances on one contour yield the same output power if selected as output impedance of the power stage. Also in this figure, the centre of the contour indicates optimum load impedance. The input and output matching networks for driver stage are conjugately matched with the inherent impedances offered by the pHEMT. These consisted of 4 stages of T and π type microstrip series transmission lines and stubs. These microstrip lines contain double metal layer for improved current carrying capacity [8]. The power and driver amplifiers have been designed with almost flat gain and reasonably suppressed reflections. Tuning the inter-stage matching network resulted in increase of delivered power up to about 14–15 dBm with a gain of 12 dB, as shown in Figure 5. Inter-stage stability (after combining the two stages) was also checked by probe pair element.

A fairly flat line gain of PA was achieved with suppressed reflection loss as shown in Figure 5. The gain is much lower than Maximum gain indicating that a compromise on gain was made to get higher power. The highest reflections are from output matching network of power stage (S_{22}) since it was not conjugate matched. This is taken care of in next section.

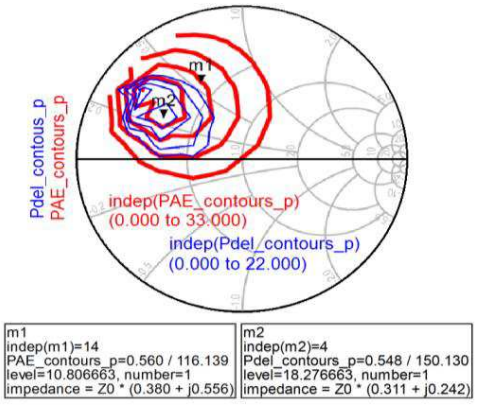

Figure 4: Power output and PAE contours on Smith chart.

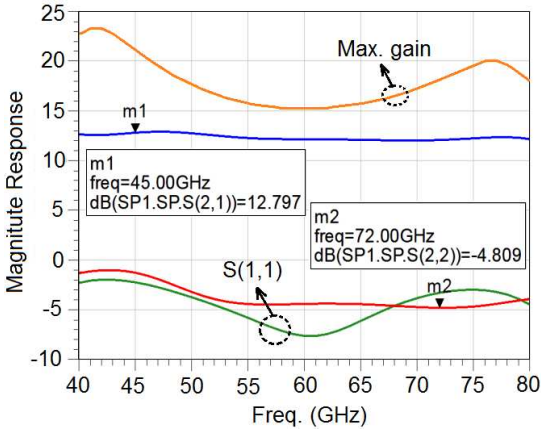

Figure 5: S-parameters of the power stage.

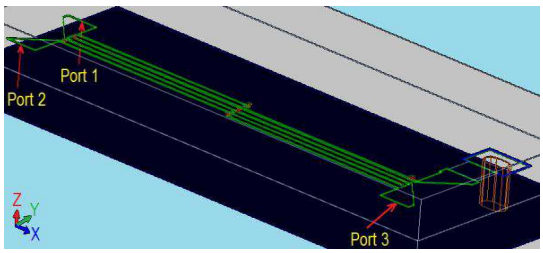

Figure 6: 2.5D simulator view of the coupler.

4. LANGE COUPLER

A four-port microstrip Lange coupler is used to operate on the frequency band of interest; i.e., 40–80 GHz. Lange coupler is selected as the most suited candidate for 3 dB quadrature coupling in monolithic substrate, since it does not need multilayer circuitry (unlike the broad-side coupler) and occupies less space on MMIC wafer (unlike branch-line coupler). Moreover, it gives 50% bandwidth around the centre frequency. The simulations were conducted using various tools of Agilent ADS 2011. The designs were also tested in Agilent Genesys and similar results were obtained. As seen in Figure 6, the implemented coupler consists of interdigitated microstrip lines placed in parallel to each other. Alternate arms are tied together with air bridges. The air bridges are implemented using special VIAS provided in the design Kit of WIN semiconductors. The isolated port is terminated with a matched thin film 50 Ω resistor and grounded; all VIAS are used in accordance with the PDK provided by WIN Semiconductors [8].

4.1. Design of Lange Coupler

The parameters used include spacing between arms, arm width, arm length (l), number of parallel arms and port width. The arm length determines the centre frequency. The coupler is effective over 50% of that center frequency (f).

$$l = \lambda/4 \tag{1}$$

$$\lambda = c/f\sqrt{\varepsilon} \tag{2}$$

where ε is effective dielectric constant of the substrate. The coupler has dimensions of 428 µm × 3.5 µm × 4.3 µm ($l \times w$, s). Narrower spacing between the arms results in tighter coupling on −3 dB level. Track widths control signal losses and thermal disspation through the microstrip. Port width was calculated to provide line impedance of 50 Ω. The coupler is designed to have four arms or digits (tested against six and eight arms during design process) to have the best tradeoff between operating bandwidth and desired coupling. The simulation response of through (Port 2)

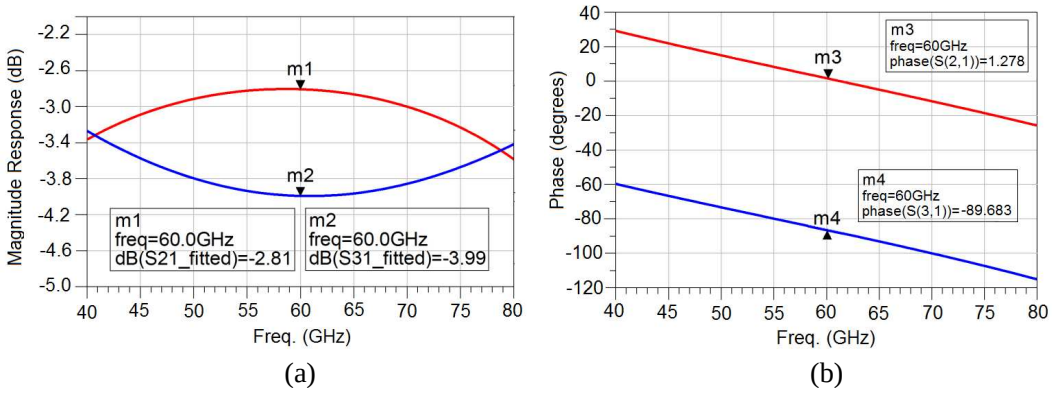

Figure 7: (a) Through and coupled port magnitudes and (b) linear phase response of quadrature coupler.

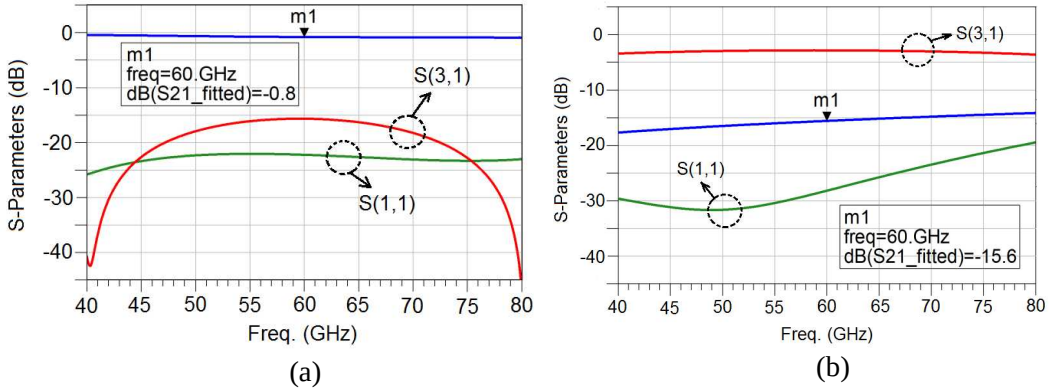

Figure 8: 2.5D Simulator results for (a) insertion loss and (b) isolation.

and coupled port (port 3) is shown in Figure 7. The coupler is designed to over-couple the signal to extend 3 dB coupling over the entire band. The variations of S_{21} (through) and S_{31} (coupled) is roughly 0.7 dB each and centered on −3 dB level. The return loss of the coupler is found to be below 20 dB over 40–80 GHz. The linearity of phase is kept in the entire bandwidth and the phase difference between two signals is maintained 90 degrees consistently. According to (1) and (2), the length should be 348 µm for 60 GHz centre frequency and a dielectric constant of 12.9. However, there is additional coupling between non-adjacent arms in the coupler and to compensate this; the length 'l' is optimised in Agilent ADS. Parameters of the designed coupler are shown in Table 1.

Vias are introduced as air bridges, with the height of each via being 2.15 µm containing 0.15 µm of SiN layer above GaAs substrate [2]. The vias used as air bridges are found to give a minimal loss of 0.013 dB.

4.2. Insertion Loss and Isolation

Insertion loss causes higher noise figure in a balanced amplifier [5]. This constitutes losses caused by the dielectric, lossy conductor and imperfect VSWR. The designed coupler is connected back-to-back to its identical unit, to couple input signal and get the recombined signal at the output. Ideally it should recover the input signal and give 0 dB loss; however, the observed output signal is between −0.4 and −0.9 dB, shown in blue in Figure 8(a). Hence, for each coupler, the insertion loss is −0.2–0.45 dB.

To determine isolation, the through port was terminated with a matched load and output (quadrature) coupled port was fed with a broad band signal. Isolation of −16 dB was observed, indicated by blue in Figure 8(b). All these tests were conducted in Agilent ADS Momentum software.

5. BALANCED AMPLIFIER

The two identical power amplifiers are placed between couplers and so, matching networks are adjusted by optimising the Microstrip stubs and TEE structures in the matching networks. The inter-stage matching network is re-adjusted after the merger so that it drops from 8 stages to 3 stages T-type (stub) matching network. The topology is shown in Figure 9.

The power output rose to a level of 16–18 dBm in the entire bandwidth. The gain was found to be same as before, i.e., 12 dB mean level and is indicated in blue in Figure 10. The reverse transmission coefficient (S_{12}) indicated in yellow, stays below −30 dB avoiding any oscillations. The output reflection coefficient (S_{22}), highlighted by red, is slightly higher than input reflection coefficient (S_{11} highlighted by green) because of the 'power-matched' condition explained above.

In given design, in order to get 18 dBm power output at its gain compression point, the input to the divider Lange coupler should be 5 dBm. For practical devices the Rollet stability factor K

Table 1: Parameters of four finger lange coupler.

Values	Dimension		
	Length	*Width*	*Spacing*
(µm)	428	3.5	4.3

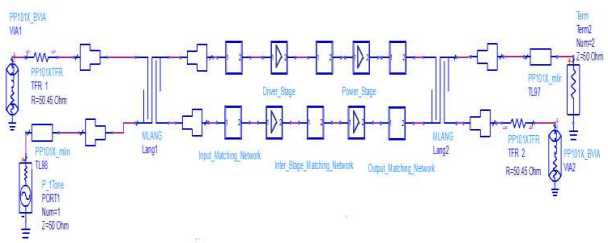

Figure 9: Power amplifiers between input and output couplers.

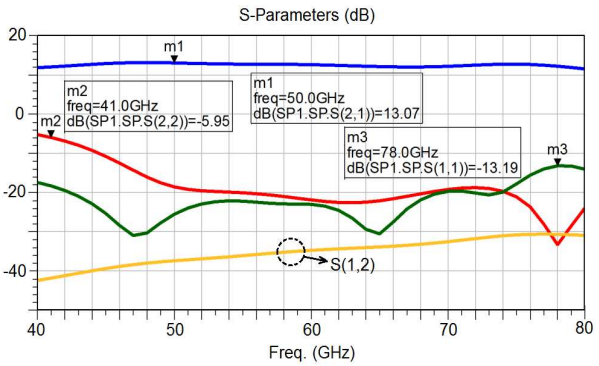

Figure 10: S-parameters of balanced amplifier.

should be greater than 1.2. In this case, gain was given a priority over stability factor. The reason is that when the amplifiers were put in balanced configuration, in between Lange couplers, then stability factor increased manifold. The reflections were absorbed by couplers' isolated port and no oscillation was possible with the new design. So while designing this amplifier, the stability was kept above 1.1 from 0 to 80 GHz. When the amplifiers were put in balanced configuration, the stability factor of overall system rose from a minimum value of 1.09 to a safe level of 3.9. The matching networks were taken to Agilent ADS 3D EM simulation to model their integration with the GaAs Design kit (PP10). The networks consist of thin microstrip series transmission lines and stubs to form pi- and T-networks. No significant differences were found in EM Modelled and 2D modelled matching networks.

6. CONCLUSIONS

A two-stage ultra-broadband millimetre-wave high power amplifier has been designed to operate in the V-band, i.e., 40–80 GHz. The coupler uses biasing technique as well as distributed effect of Lange coupler, to ensure stability and high gain and power transfer of the system. The gain and power pattern over the entire bandwidth is consistent and flat with inherent stability of the whole system. The results from both simulation software were found consistent and it is expected that measurement results will be the same. The port impedances of the Lange coupler are set to a standard of 50 Ω so that it can be easily integrated to networks designed for other applications. Overall, the proposed amplifier is a good candidate for mm-wave applications and instrumentations.

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