An Optimized Opamp-sharing in 2nd Order $\Delta\Sigma$ Modulator Based on Changing the Stages Output Capacitance Timing Strategy

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Abstract— In this paper a new approach to OPAMP sharing was proposed. In this way, the pulse-width dedicated is proportional to output capacitance. Consequently, the created harmonic distortion is minimized and the power efficiency is maximized.

1. INTRODUCTION

Delta-sigma modulators are very used in the Control loop of the DC-DC Switching Converters that tabernacle with PWM generators and decreases the ripple and noise of the DC-DC converters [1]. In fact these modulators covert analog input signal $U(z)$ to a digital representation $Y(z)$. The difference between output digital signal and input analog signal of modulators is so called quantization error $E(z)$. Quantization error is known as noise which limits analog to digital modulators accuracy. In this type of modulators, the quantization noise is fed back to the input of the modulator and being attenuated while passing through loop filters. In addition, any other noise sources which are located in the forward path of the modulator could be attenuated by this technique of fed back the noise signals to the input. Attenuating quantization noise causes an increase in accuracy of the modulator Concept of a conventional delta sigma modulator is shown in Figure 1.

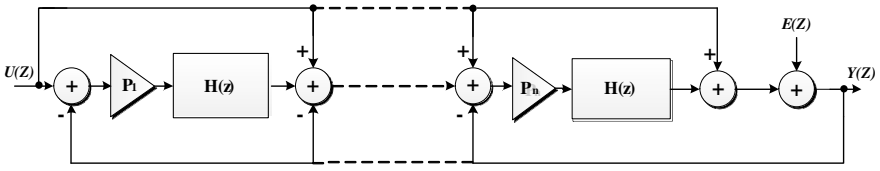

Figure 1: The conventional nth order delta sigma modulator.

The signal transfer function $S_{TF}(z)$ and noise transfer function $N_{TF}(z)$ of the delta sigma modulator is as the following:

$$Y(Z) = (1 - Z^{-1})^n E(Z) + U(Z) \tag{1}$$

$$\begin{cases} S_{TF}(Z) = \frac{Y(Z)}{U(Z)} = 1 \\ N_{TF}(Z) = \frac{Y(Z)}{E(Z)} = (1 - Z^{-1})^n \end{cases} \tag{2}$$

In the conventional delta sigma modulators, increasing forward path filters more than 3 usually leads to instability [2]. There has been introduced many techniques which provide the same noise transfer function and signal transfer function as the conventional has for the high order noise shaping by mathematical techniques [3–5].

In this paper, a new approach to opamp-sharing has been introduced in which provides a second order noise shaping by moving opamp between two stages.

The paper has been organized as the following. Next section describes the conventional noise shaping method and it has been followed by the proposed noise shaping method. Finally the paper presents the second order modulator simulation results.

2. CONVENTIONAL NOISE SHAPING METHOD

An important of ideas for decreases of the power consumption and area is opamp-sharing. In this technique, opamp moved from stage1 to stage2 and conversely. In conventional idea, two phases are used that the pulse width dedicated to phases are the same. But the stage output capacitance (i.e., equal the whole capacitances in one integrator in a stage) in stage1 is more than stage2, because

the stage1 once shaped the noises while the stage2 twice shaped the noises. Therefore the stage2 needed to pulse-width (i.e., phase pulse-width) less than stage1. Pulse-width dedicated to phases in conventional noise shaping method shown in Figure 2.

If the pulse-width dedicated to stages of delta-sigma modulator has been the same while the output capacitances of the stages are different, with moving the opamp between the stages, the harmonic distortions are increases and resultant the SNDR is decreases Therefore with this technique, for struggle the harmonic distortions should be increase the sampling frequency that the phase1 pulse-width increases. Therefore power consumption and chip area are increases.

3. PROPOSED NOISE SHAPING METHOD

According to discussion in Section 2 for opamp-sharing technique should be the pulse-width dedicated to stages is designed according to stages output capacitance.

In this design, we effort that the pulse-width dedicated to stages have been based on stages output capacitance. Timing diagram for the proposed noise shaping method seen in Figure 3.

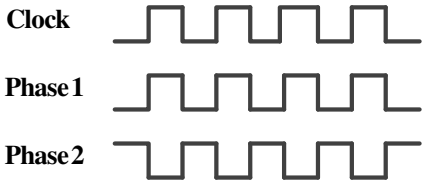

Figure 2: Timing diagram for conventional noise shaping method.

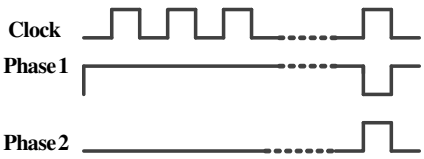

Figure 3: Proposed noise shaping method timing diagram.

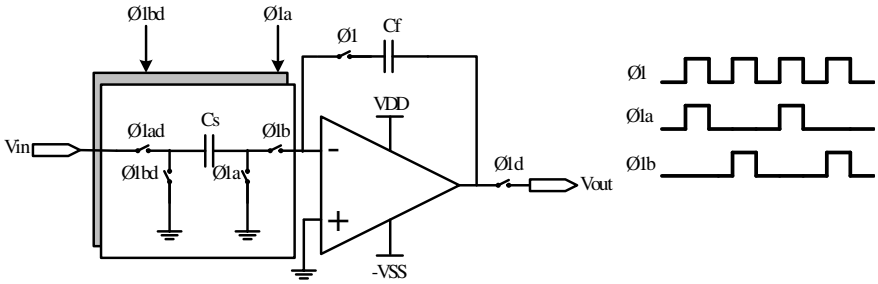

Figure 4: Proposed Switch-Capacitor Integrator in phase1 (Φ1).

According to Figure 3, the pulse-width dedicated to stage2 is less than stage1 and the phases are madding from the clock signal with very high frequency rather than two phases. With this technique, the power dissipation and chip area minimized by factor about two.

The proposed integrator structure shown in Figure 4. In this structure, the opamp only required in one phase and it can move to other stages. According to Figure 4 based on [6], in the phase Φ_{1a}, the integrator sampled the input signal on the sampling capacitor (C_S) and in the phase Φ_{1b}, the integrator transfer the electric load from sampling capacitor to integrator capacitor (C_f) and conversely. Therefore, the opamp not require been in the integrator structure at phase2 and moved to other integrator.

4. SIMULATION RESULTS

In this paper, the proposed block diagram in Figure 5 is simulated. According to Figure 5, the opamp has been in stage1 at phase1 (Φ1) and the opamp has been in the other stage at phase2 (Φ2). The output capacitance of the stage1 is about six times than stage2. Therefore, the pulse-width for stage1 is about six times other stage.

The proposed idea simulated at the 130 nm CMOS model and the comparison between State-of-the-Art Works between the proposed paper results and some other papers presented at the Table 1. According to this table, the proposed SNDR and power consumption are 80.7 dB and 69.2 µw respectively, resultant FoM equal 392.2 fJ/step-conv that higher than other papers.

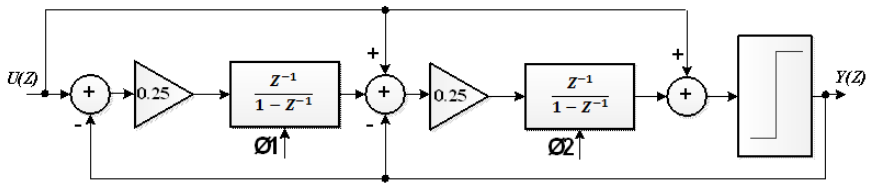

Figure 5: Proposed 2nd order delta-sigma modulator block diagram.

Also, Table 2 shows the simulation results in the process corners. According to this table, the tolerance between T.T corner and other corners for the SNDR is less than 10%, that an appropriate error of engineering.

Table 1: Comparison to State-of-the-Art works.

Parameters	**[7]**	**[8]**	**[9]**	**[10]**	**This Work**
V_{DD} **(v)**	0.9	1.4	1.2	0.9	**1.2**
CMOS Technology (nm)	180	180	130	65	**130**
f_{BW} **(Hz)**	10 k	256	10 k	500	**10 k**
Order	2	2	2	2	**2**
SNDR (dB)	80.1	72	87.8	76	**80.7**
Power (μw)	200	13.3	148	2.1	**69.2**
FoM (fJ/step-conv)	1210	7980	369	407	**392.2**

Table 2: Simulation results for the proposed 2nd order ΔΣ at different process corners.

Parameters	**T.T**	**S.S**	**S.F**	**F.S**	**F.F**
f_{BW} **(Hz)**	10 k	10 k	10 k	10 k	10 k
SNDR (dB)	80.66	81.85	78.70	80.21	78.23
ENOB (bit)	13.11	13.30	12.78	13.03	12.70
FoM (fJ/s-c)	392.25	295.79	540.16	385.39	648.44

5. CONCLUSION

In this paper, a new approach to OPAMP sharing was proposed. In this way, the pulse-width dedicated is proportional to output capacitance. Consequently, the created harmonic distortion is minimized and the power efficiency is maximized. In this design, in one 2nd stage delta-sigma modulator with 10 kHz of bandwidth, the power dissipation equal of 69.2 μw, resultant the FOM is 392.2 fJ/step.

REFERENCES

1. Alghamdi, M. K. and A. A. Hamoui, "A spurious-free switching buck converter using a delta-sigma modulation controller with a scalable sampling frequency," *IEEE J. Solid-State Circuits*, Vol. 47, 841–851, Feb. 2012.
2. Johns, D. and K. Martin, *Analog Integrated Circuit Design*, Wiley, New York, 1997.
3. Malcovati, P., et al., "Behavioral modeling of switched-capacitor sigma-delta modulators," *IEEE Trans. Circuits Syst. I*, Vol. 50, 352–364, Mar. 2003.
4. Cannillo, F., et al., "1.4 V 13 W83dBDRCT-modulator with dual-slope quantizer and PWM DAC for biopotential signal acquisition," *Proc. ESSCIRC*, 267–270, Sep. 2011.
5. Nilchi, A. and D. A. Johns, "A low-power Delta-Sigma modulator is using a charge-pump integrator," *IEEE Trans. Circuits Syst. I*, Vol. 60, 1310–1321, May 2013.

6. Yao, L., M. S. J. Steyaert, and W. Sansen, "A 1-V 140-µW 88-dB audio sigma-delta modulator in 90-nm CMOS," *IEEE J. Solid-State Circuits*, Vol. 39, 1809–1818, Nov. 2004.
7. Goes, J., B. Vaz, R. Monteiro, and Paulino, "A 0.9 V modulator with 80 dB SNDR and 83 dB DR using a single-phase technique," *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 74–75, Feb. 2006.
8. Cannillo, F., et al., "1.4 V 13 W83dBDRCT-modulator with dual-slope quantizer and PWM DAC for biopotential signal acquisition," *Proc. ESSCIRC*, 267–270, Sep. 2011.
9. Nilchi, A. and D. A. Johns, "A low-power Delta-Sigma modulator is using a charge-pump integrator," *IEEE Trans. Circuits Syst. I*, Vol. 60, 1310–1321, May 2013.
10. Yeknami, A. F., et al., "Low-power DT $\Delta\Sigma$ modulators using SC passive filters in 65 nm CMOS," *IEEE Trans. Circuits Syst. I*, Vol. 61, 358–370, Feb. 2014.