Real-time Processing Technique for Panoramic Infrared Imaging System

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Abstract— Panoramic infrared imaging system (PIIS) based on the long linear array long-wave detector is introduced. Due to the real-time processing and high-speed data transfer demanding, we propose a high-performance processing platform based on field programmable gate array (FPGA) + multicore digital signal processor (DSP) architecture. To reduce the platform's power consumption, dynamic power monitoring technology is used to provide variable core voltage management for DSP. Then mapping an application to the platform is illustrated, which is guided by parallel-task segmentation mechanism of multi cores system. We show that, the designed platform with the optimization strategies achieves powerful capabilities of data throughput and processing performance.

1. INTRODUCTION

Infrared imaging has abilities of passive detection, well anti-jamming and work double tides. Using infrared sensors to implement region searching and early warning, has become an important target surveillance method. To increase detection distance and accuracy of searching system for, the searching field of view (FOV) should expand as large as possible. In addition, with applications of infrared imaging in areas such as space remote sensing, multi-target surveillance and satellite-to-ground reconnaissance, the development of high-performance detector with high-resolution, large FOV and great quantities of image elements has become the urgent demand.

There are two methods to improve the detection FOV for infrared detectors at present [1]: one is to develop large area focal plane array (FPA), which is complex and high cost; another is to develop long linear array FPA (defining more than 480-elements as long linear array). Considering the factors of material, process technology and so on, obtaining long linear array through splicing short ones, is low cost and able to produce more than 1000-elements [2, 3]. In the year 2010, H. B. Fan [4] developed the 1152×6 long wave linear array, and implemented the infrared searching system for 1152×50000 high-resolution panoramic imaging.

Computing performance of image processing platform is crucial to the PIIS, which performs complex operations of $50000 \times 1152 \times 8$ bit size of raw data, such as panoramic image display, image enhancement and target detection.Thereby an efficient platform must have capabilities of high-speed data transfer and real-time processing. This paper addresses the high-speed processing platform design and performance optimization, based on Fan's imaging system engineering application.

2. PANORAMIC INFRARED IMAGING SYSTEM

The 1152×6 linear array long wave infrared detector [4] is utilized to compose the panoramic imaging system in our approach. The long linear array is achieved by the following steps: two 288×6 linear array modules are parallelly arranged in the horizontal direction, constituting one 576×6 array to increase the resolution. Then, two 576×6 array modules cascade again in the vertical direction, thereby increasing the FOV. Imaging system gets the panoramic view through the continuously scanning in horizontal direction of the long linear array detector.The whole system consists of infrared scanning head, image display and control unit, servomotor and so on, a picture of its structure shown in Fig. 1.

Installed in the servomotor, the step searching in pitching direction is through pitching control mechanism regulating the main reflector, while in azimuth direction through the linear array uniformly rotating one cycle per second to cover nearly 360 degrees searching range. The 50000 columns detection data produced in one revolution of the linear arrays are arranged column by column. The imaging system outputs up to 50000×1152 pixels per frame, which provides large enough FOV of high-resolution and high-definition panoramic image for searching. The main technical parameters of the system are as follows: 1) Detection capability: 360 degrees search per second. 2) FOV: $360^\circ \times 4^\circ$ panoramic view. 3) Detector: 288×6 long wave cooled detector. 4) Output image sizes: 288×50000, 576×50000, 1152×50000. 5) Frame frequency: 1 Hz.

Figure 2 shows a full frame of the real panoramic image. Because the actual size is too large to fit display, the whole image is divided into eight parts equally and compressed along the horizontal direction, with each part covering 45 degrees range.

Figure 1: A picture of the panoramic imaging system.

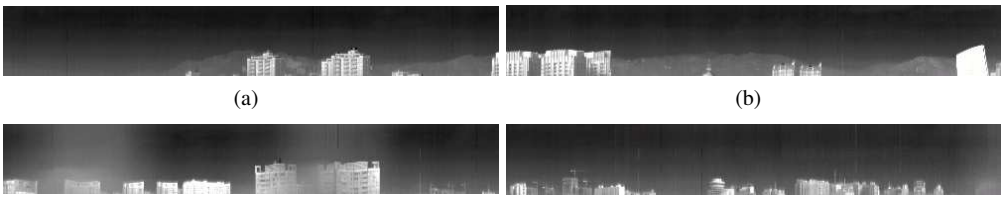


Figure 2: Total frame display of the real panoramic infrared image: part 1–4.

3. HARDWARE IMPLEMENTATION OF THE PROPOSED REAL-TIME PROCESSING PLATFORM

3.1. FPGA+DSP Architecture Design

In order to guarantee real-time, the total 54.9 MByte data acquired from the PIIS requires to be processed in one second and synchronously transferred to the display terminal. Further, the storage resources, computing speed and high-speed data transfer also should be taken into account. Texas Instruments (TI) has developed the industry's first 10 GHz multicore DSP TMS320C6678 in 2010 [5], with integrated fixed- and floating-point performance. Based on the innovative keystone architecture, the device has eight 1.25 GHz C66x cores providing 320 Giga-multiply accumulate per second (GMACs) and 160 Giga-floating point operations per second (GFLOPs) of performance. With flexible programmable ability and plenty of on-chip logic cells, FPGA devices integrate the power-efficient transceiver rocket IO with line rate up to 10 Gbps [6], which is the most suitable carrier to realize high-speed interconnection.

Based on industry's latest generation of multicore fixed- and floating-point DSP, and the high-performance FPGA, this paper designs a mix architecture of FPGA and DSP, to provides vast processing power for the PIIS, which has the following advantages: 1) Maximizing the throughput of on-board data flows and eliminating the performance bottlenecks. 2) Complex data computing by DSP, and programmable and reconfigurable resources of FPGA fully employed. 3) Hardware modules with portability and expansibility, that is ease to form more complex system and improve the performance. 4) Utilizing multi cores of single DSP to set up parallel system, yielding optimized parallelism while greatly simplifying the circuit for miniaturization and low power consumption.

Hardware block diagram of the real-time processing platform is shown in Fig. 3(a). The PCB board of the proposed platform shown in Fig. 3(b) is standard height and full-length x8 add-in card. It integrates a Virtex-6 family LX240T FPGA and a TMS320C6678 multicore DSP, that is efficient to accomplish complex algorithm for large volumes of data by parallel processing. Large-capacity DDR3 dynamic memory, the flexible depth expansion SODIMM and flash memory, yield real-time caching and high-speed fetch and load. In addition, complex system setting up and multi devices management is facile with abundant peripherals on the board.

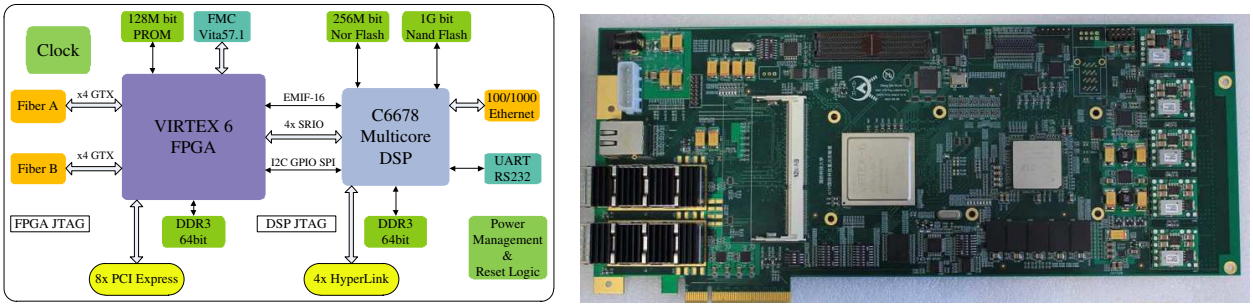


Figure 3: The proposed real-time processing platform. (a) Functional block diagram. (b) The PCB board.

3.2. Low Power Consumption: Variable Core Supply Voltage

In practical, some optimization measures can be taken to maximize the platform performance in terms of hardware design and program development. This section presents a methodology of low power consumption of DSP through the dynamic power monitoring technology. In order to decrease the power consumption while maintaining the device performance, TI developed a variable core supply solution, called SmartReflex technology [7]. It is able to dynamically monitor the power change and allows the core voltage to be optimized based on the device process corner.

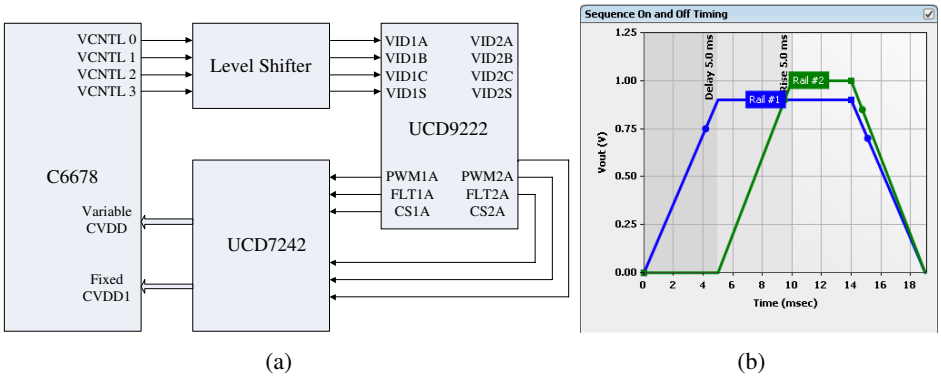


Figure 4: The variable and fixed core supply design for c6678 DSP, (a) Schematic circuit diagram. (b) On and off timing of the two power rails.

This paper uses a dual digital controller UCD9222 and a dual synchronous-buck power driver UCD7242 to regulate the DSP's core supply voltages: the variable core rail CVDD and the fixed 1.0 V core rail CVDD1. Fig. 4(a) is the schematic diagram designed for the DSP core power supply of our board, where one output of UCD9222 controller regulates the variable core rail, and the other unused output is configured as the fixed power rail. Fig. 4(b) shows the on and off timing of two core supply, where the blue curve represents the variable rail CVDD timing while the green curve represents the fixed rail CVDD1 timing.

In order to verify the validity of the hardware design and software configuration, real-time monitoring is applied to the two power rails by the UCD device design tool of fusion digital designer (Fusion GUI). Actual state on the board is read and displayed in Fig. 5. Take example for CVDD rail results shown in Fig. 5(a), the six windows on the right side are real timing of key parameters: input voltage Vin, input current Iin, output voltage Vout, output current Iout, output power Pout and the maximum temperature Temp. It can be seen clearly that, all the parameters fluctuate within the expected range, not exceeding the yellow warning curve and red error curve. This demonstrates that the hardware design in Fig. 4(a) realizes the SmartReflex technology for C6678 core supply. In addition, the two windows on the left side list the acquired information. The above one is the latest value in the "Readings group". The nether one displays the status register, where the green "OK" marks the correct state while the red "Fault" marks the wrong state.

(a) (b)

Figure 5: Live parameters monitoring for the power rails: (a) CVDD, (b) CVDD1.

4. PLATFORM PERFORMANCE TESTS:HIGH-BANDWIDTH TRANSFER

To demonstrate the capability of high-bandwidth transfer with the designed platform, we select SRIO as an example to test. Different kinds of affairs and loads can influence the transfer speed greatly. Fig. 6 plots the curves of transfer speed for several affairs with various loads. As the load increasing, packet overhead of the SRIO protocol decreases, so the speed approximates theoretical value (1.25 GBps). When the packet load is small, affair of "Message" have the longest response time thereby the slowest rate. When the packet load is large, affair of "Nread" has the longest response time thereby the slowest rate.

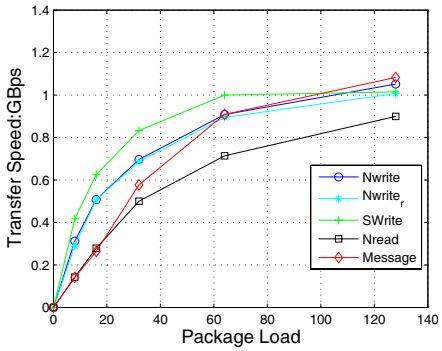


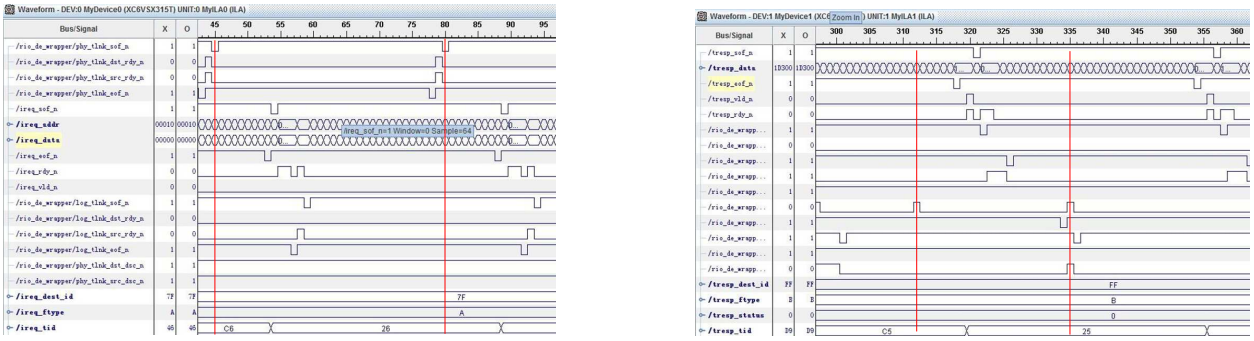
Figure 6: Transfer rate of different packages.

With maximum transfer rate set to 5 Gbps, the FPGA is used as initiator while DSP as the destination to test actual transfer rate by the SRIO protocol. Writing process is tested by sending "Swrite" packets from FPGA to DSP. On the other hand, FPGA sends "Nread" packets to DSP while DSP returns response packets to FPGA, which performs reading test. Using the ChipScope to capture continuous execution of SRIO reading and writing, the timing results are shown in Fig. 6 and Fig. 7 respectively. The average time interval by using FPGA as initiator endpoint to receive response packets (load 256 Byte) is 144 ns (36 clock cycles as the distance between the two red lines), whose transfer rate is 1.78 GBps. Similarly, the average time interval by using FPGA as destination endpoint to receive "Nread" packets (load 256 Byte) is 144 ns (35 clock cycles as the distance between the two red lines), whose transfer rate is 1.83 GBps.

Then we calculate the theoretical transfer rate and further analyze actual communication efficiency of SRIO reading and writing under the above experimental conditions. FPGA sending each "Swrite" packet will cost overhead of ten bytes, and the DSP returns a four-byte symbol to affirm reception. Therefore the theoretical transfer rate of SRIO writing data is calculated as

$$2.0\,\mathrm{GB/s} \times \frac{256}{256+10+4} = 1.896\,\mathrm{GB/s} \tag{1}$$

DSP returns each response packet which costs overhead of eight bytes, and also returns a four-byte symbol of affirming reception while receives the "Nread" packet. In addition, FPGA will also



(a) (b)

Figure 7: The real timing of SRIO rate: (a) FPGA writing data to DSP, (b) DSP writing data to FPGA.

return a four-byte symbol while receives the response packet. So the theoretical transfer rate of SRIO reading operation is given by

$$2.0\,\text{GB/s} \times \frac{256}{256+8+4+4} = 1.882\,\text{GB/s} \tag{2}$$

The actual communication efficiency of SRIO writing operation and SRIO reading operation are final calculated as

$$frac1.83\,\text{GB/s}1.896\,\text{GB/s} \times 100\% = 96.5\% \tag{3}$$

$$frac1.78\,\text{GB/s}1.882\,\text{GB/s} \times 100\% = 94.5\% \tag{4}$$

The testing results show that, the actual communication efficiency of SRIO approaches theoretical value. But the longer time by which DSP responses to FPGA reading request, causing a lower efficiency of reading operation.

5. CONCLUSION

The PIIS has abilities of panoramic FOV covering 360-degree airspace, high-resolution and multi-elements. This article addresses the real-time processing technique of image acquisition and panoramic display of the PIIS. It proposed a high-performance processing platform based on the FPGA + multicore DSP architecture. Using the dynamic power monitoring technology, the problem of high power consumption in circuits with high clock rate and complex device is solved effectively. The designed platform and optimization methodology make the high speed data transfer and real-time processing in PIIS possible and realizable.

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