A High-Q Linear CMOS Digitally Controlled Accumulation-mode Varactor Array for Multiband RF Circuits

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Abstract— Electronically tunable capacitors are key elements for tunable and reconfigurable RF circuits. The most popular tunable capacitor topologies in CMOS are the analog varactor and digitally controlled switched capacitor array (SCA). The conventional analog varactor shows a high quality factor (Q-factor) in both the minimum capacitance ($C_{\min}$) and the maximum capacitance ($C_{\max}$) states with a wide tuning range, but it has a poor linearity performance due to the voltage dependent nonlinear capacitance. In case of the digitally controlled SCA, while it shows a very good linearity, its Q-factor in $C_{\min}$ state is strongly dependent on the substrate loss by the parasitic junction capacitances between P-well, deep N-well, and P-substrate and the substrate resistance. Especially, if the SCA is implemented in a standard digital CMOS process without deep N-well, it suffers from severe Q-factor degradation in $C_{\min}$ state at higher frequencies. In order to overcome the aforementioned drawbacks of the analog varactor and the digitally controlled SCA, the digitally controlled binary-weighted accumulation-mode varactor array (AVA) is proposed. Contrast to the conventional analog varactor tuned by continuous analog voltage, the proposed AVA uses only two states of $C_{\min}$ and $C_{\max}$ of the analog varactor by digitally on/off control. Instead of a zero voltage reference, the negative voltage ($-VDD$) is applied to the gate of the analog varactor in $C_{\min}$ state in order to maximize the tuning range, power handling capability, and linearity. The total capacitance varies by turning on ($+VDD$) or off ($-VDD$) each branch of the proposed AVA. The proposed AVA keeps a high Q-factor in all states even if it is implemented in a standard digital CMOS process without deep N-well, while showing comparable linearity performance in comparison with the conventional SCA. In simulation, Q-factor at 2.4 GHz is greater than 70 over all states and the tuning range is about 3.1.

1. INTRODUCTION

The integrated tunable capacitor with large a tuning range ($T.R.$), a good linearity, and a high Q-factor is an essential building device for multi-band (MB)/multi-mode (MM)/multi-standard (MS) tunable RF circuits, because it directly affects the key RF performances such as frequency tuning range and phase noise of the voltage-controlled oscillators (VCOs), power efficiency of the tunable power amplifiers (PAs), and noise figure (NF) and linearity of the tunable low noise amplifiers (LNAs) and tunable filters. Especially, in order to preserve maximum filed length andpower efficiency of the PAs under the condition of antenna impedance mismatch, it is very important to implement high-Q tunable capacitors in designing the tunable impedance matching circuits.

The most popular tunable capacitor topologies in CMOS are the analog MOS varactors in Fig. 1(a) and digitally controlled switched capacitor array (SCA) in Fig. 2(a)Concerning the analog MOS varactors, there are two types of MOS varactors. One is the accumulation-mode varactor and the other is the inversion-mode varactor. Typically, the accumulation-mode varactor shows better $T.R.$ and Q-factor values than the inversion-mode varactor [1, 2]. Unfortunately, however, both topologies show a poor linearity performance due to the voltage dependent nonlinear capacitance. When they are in depletion region, the linearity of the MOS varactors is severely degraded.

Concerning the digitally controlled SCA in Fig. 2(a), it is constructed with several switched capacitor branches in parallel, each of which consists of a unit capacitor in series with NMOS transistor as a digital switch. The unit capacitors in each branch are designed to bebinary-weighted to minimize the number of branches, and the channel widths of transistors are also binary-weighted to keep the same Q-factor. The state-of-the-art techniques such as floating gate (body) method and negative biasing method are commonly applied in order to increase the power handling capability of the digitally controlled SCA. By digitally controlling the gate and the body of NMOS transistors, the total capacitance can be controlled while maintaining good linearity. However,its Q-factor in $C_{\min}$ state is strongly dependent on the substrate loss by the parasitic junction capacitances between P-well, deep N-well, and P-substrate and the substrate resistance. Especially, if the SCA is implemented in a standard digital CMOS process without deep N-well, it suffers from severe Q-factor degradation in $C_{\min}$ state at higher frequencies.

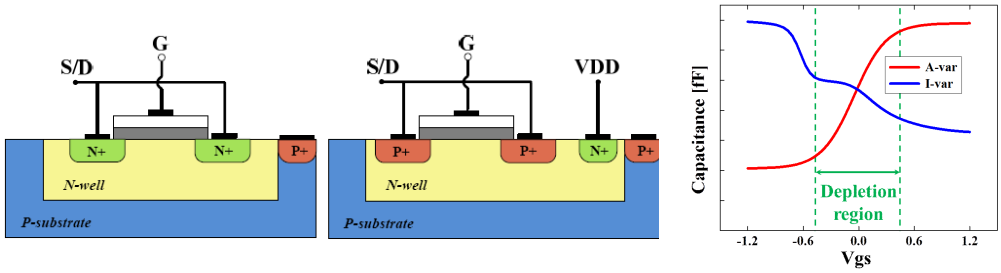


Figure 1: (a) Cross-sectional view of MOS varactors (left side: accumulation-mode varactor, right side: inversion-mode varactor); (b) their capacitance-voltage (C-V) characteristics.

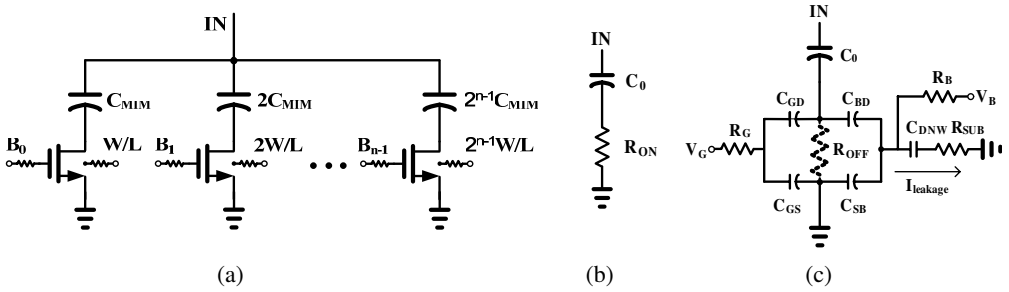


Figure 2: (a) Digitally controlled SCA with a resistive floating technique; (b) its simple equivalent circuit in the on-state; (c) its simple equivalent circuit in the off-state.

In this paper, the effect of the parasitic junction capacitances and substrate resistance on Q-factor of the digitally controlled SCA is studied. In addition, the digitally controlled binary-weighted accumulation-mode varactor array (AVA) is proposed in order to overcome the linearity and Q-factor degradation of the analog MOS varactor and digitally controlled SCA, respectively.

2. ANALYTICAL STUDY ON EFFECT OF PARASITIC JUNCTION CAPACITANCES AND SUBSTRATE RESISTANCE ON Q-FACTOR OF DIGITALLY CONTROLLED SCA

For the on-state NMOS transistors, the floating gate (body) method is adopted in order to keep constant turn-on state of the transistors and turn-off state of the junction diodes irrespective of the signal power [3]. On the other hand, for the off-state NMOS transistors, the negative biasing method is applied in order to prevent the undesirable channel formation in the event of a large signal input and improve the power handling capability [4]. It also increases $T.R.$ of the digitally controlled SCA by reducing $C_{\min}$. Figs. 2(b) and (c) show the simple equivalent circuits of 1-bit SCA with a resistive floating technique in triple-well CMOS process in the on-state and off-state, respectively. Compared to the on-state mode, the parasitic junction capacitances (C_{DNW}) between P-well, deep N-well, and P-substrate and the substrate resistance (R_{SUB}) in Fig. 3 greatly degrade Q-factor of NMOS transistor in the off-state.

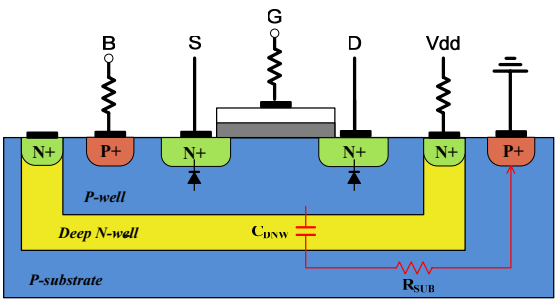


Figure 3: Cross-sectional view of NMOS transistor in a triple-well structure.

Figure 4 shows a more detailed schematic for 3-bit SCA including shunt paths from body to AC ground, which consists of C_{DNW} and R_{SUB}. Based on the measured data in [5], the values of

C_{DNW} and $R_{SUB}$is adjusted according to the transistor dimension.

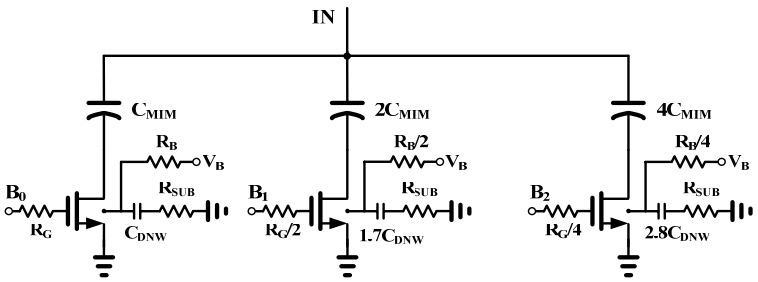


Figure 4: A more detailed schematic for 3-bit SCA including shunt paths from body to AC ground.

Figure 5(a) shows the simulated Q-factor and $T.R.$of 3-bit SCA at 2.4 GHz according to the variation of R_{SUB}. In simulation, C_{DNW} in LSB branch is assumed to be 65 fF. The Q-factor in $C_{\min}$ state of 3-bit SCA is strongly dependent on the magnitude of R_{SUB}, whereas $T.R.$ is almost constant over R_{SUB}. Fig. 5(b) presents the simulated Q-factor in $C_{\min}$ state of 3-bit SCA according to the variation of C_{DNW} and R_{SUB}. From Fig. 5(b), we know that Q-factor in $C_{\min}$ state can be improved by either increasing or decreasing substrate resistance. Because the resistivity of the substrate in a standard CMOS process ranges from 10 to 100 Ω-cm, it is very difficult to achieve substrate resistance R_{SUB} of greater than 1 KΩ by only control ofthe substrate contact. Therefore, it is desirable to choose low substrate resistance by placing ground contacts as close as possible to the N-well area of the NMOS transistor. Typically, low substrate resistanceR_{SUB} in a standard CMOS process ranges from 50 to 300 Ω [5, 6]. In conclusion, considering typical values of C_{DNW} and R_{SUB}, the degradation of Q-factor in $C_{\min}$ state of the digitally controlled SCA is inevitable. In a standard digital CMOS process without deep N-well (the case for C_{DNW} of 100 pF in Fig. 5(b)), Q-factor in $C_{\min}$ state is severely degraded.

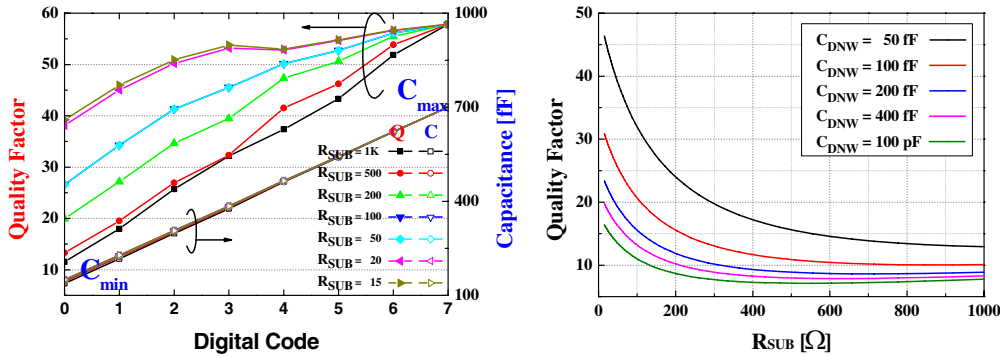
3. DESIGN OF PROPOSED DIGITALLY CONTROLLED ACCUMULATION-MODE VARACTOR ARRAY (AVA)

In order to overcome the linearity and Q-factor degradation of the analog MOS varactor and digitally controlled SCA, the digitally controlled binary-weighted accumulation-mode varactor array (AVA) is proposed as shown in Fig. 6. It is constructed with several accumulation-mode varactor branches in parallel. Compared to the digitally controlled SCA, the capacitance of the metal-insulator-metal (MIM) capacitor in each branch of the proposed AVA is much larger than that of the accumulation-mode varactor. That is, it works as a bypass capacitor. Contrast to the conventional analog varactor tuned by continuous analog voltage, the proposed AVA uses only two states of $C_{\min}$ and $C_{\max}$ of the analog varactor by digitally on/off control. Instead of a zero voltage reference, the negative voltage ($-VDD$) is applied to the gate of the analog varactor in $C_{\min}$ state in order to maximize $T.R.$, power handling capability, and linearity. The total capacitance varies by turning on ($+VDD$) or off ($-VDD$) each branch of the proposed AVA. This on/off control for the accumulation-mode varactors ensures a good linearity. Note that the proposed topology fundamentally eliminates the problem of Q-factor degradation in $C_{\min}$ state of the conventional SCA, because it is free from the leakage through the parasitic junction capacitances and substrate resistance.

Table 1 summarizes the performance metrics simulated herein for the proposed AVA and compares them to those of conventional SCA. In simulation, Q-factor at 2.4 GHz of the proposed AVA is greater than 70 over all states and the tuning range is about 3.1. Compared to the conventional SCA, it greatly improves Q-factor in $C_{\min}$ state without any degradation of other performances.

Table 1: Simulated performance summaries of proposed AVA and comparison to conventional SCA.

Topologies	$C_{\min}$ ($B_0B_1B_2 = 000$)	$C_{\max}$ ($B_0B_1B_2 = 111$)	$T.R.$	Q-factor ($C_{\min}$)	Q-factor ($C_{\max}$)
SCA (3 bit)	147 fF	700 fF	4.8	16.6	57.8
AVA (3 bit)	226 fF	703 fF	3.1	127.2	73.3



(a) (b)

Figure 5: (a) Simulated Q-factor and $T.R.$ of 3-bit SCA at 2.4 GHz according to the variation of R_{SUB}; (b) simulated Q-factor in $C_{\min}$ state of 3-bit SCA according to the variation of C_{DNW} and R_{SUB}.

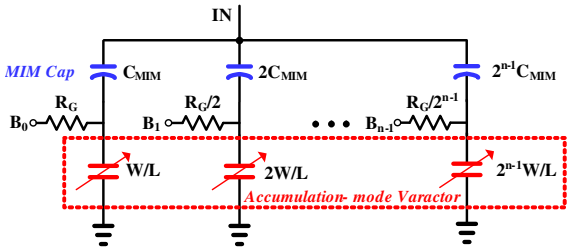


Figure 6: Proposed digitally controlled accumulation-mode varactor array (AVA).

4. CONCLUSIONS

In order to overcome the linearity and Q-factor degradation of the analog MOS varactor and digitally controlled SCA, the digitally controlled binary-weighted accumulation-mode varactor array (AVA) is proposed. The proposed AVA keeps a high Q-factor in all states even if it is implemented in a standard digital CMOS process without deep N-well, while showing comparable linearity performance in comparison with the conventional SCA. In simulation, Q-factor at 2.4 GHz is greater than 70 over all states and the tuning range is about 3.1.

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