

Analysis and Design of a Wideband Low Phase Noise LC VCO

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Abstract— In this paper, a LC voltage-controlled oscillator (LC-VCO) design optimization methodology based on switchable capacitor array is presented. The study of the compromises between phase noise and tuning range permits optimization of the design for given specifications. According to analytical phase noise models and tuning range, it allow to get a design space map where the design tradeoffs are easily identified. The proposed VCO is designed with the proposed methodology and implemented in SMIC's 0.18- μm RF CMOS technology and the chip area is $650\text{ }\mu\text{m} \times 500\text{ }\mu\text{m}$, including the test buffer circuit and the pads. Simulation results show that its tuning range is 36.4%, from 4.5 to 6.5 GHz. The simulating phase noise is -112.8 dBc/Hz at 1 MHz offset from the 6.5 GHz carrier. The maximum average power consumption of the core part is 6.47 mW at 1.8 V power supply.

1. INTRODUCTION

With the development of wireless communication technology, multi-standard portable terminals become a research focus. the RF front-end should be compatible with various wireless communication standards covering the frequency range from several hundred kHz to several GHz. Thus, the large tuning range and low phase noise wideband VCO becomes more and more important.

It is common that a CMOS VCO uses a varactor-tuned LC resonator and the ratio of the maximum to minimum capacitance of a typical varactor in CMOS technology is around 4–6, which in turn limits the frequency tuning range to a ratio of approximately 2–2.5 [1]. To extend the tuning range, the LC-tank VCO may employ a switchable capacitor array [2–8] or inductor array [9, 10]. Moreover, inductor array needs larger areas than the capacitor array and isn't suitable for the oscillating frequency below 10 GHz. Thus LC-VCO with a switchable capacitor array has been applied more widely.

The tuning range and phase noise of the LC-VCO, with switchable capacitor array, have been degraded by the switch parasitic capacitance and loss. In this paper, the relationship between phase noise and tuning range can be analyzed based on switchable capacitor array. The tradeoffs between phase noise and tuning range permits optimization of the design is discussed. A LC-VCO is implemented in SMIC's 0.18- μm RF CMOS technology. The theoretical analysis results have been verified by the simulation results.

2. CIRCUITS DESIGN

2.1. Analysis of Tuning Range

The oscillating frequency of LC-VCO is determined by LC tank. The equivalent circuit of the LC tank with a switchable capacitor array is shown in Fig. 1. Thus, the oscillation frequency of LC-VCO is given by

$$f_{osc} = \frac{1}{2\pi\sqrt{L\left(\frac{C_v}{2} + C_{array} + C_{para}\right)}} \quad (1)$$

where C_v and C_{array} are the capacitance of the varactor and switchable capacitor array, respectively; C_{para} is the parasitic capacitance. The change range of the LC-VCO oscillating frequency is controlled by the capacitance of the capacitor array and varactors. The capacitance of varactors, controlled by the controlled voltage (V_C), is so small that the change rate of the LC-VCO oscillating frequency is not enough large. Thus, the large tuning range mainly depends on the capacitor array. Under the general conditions, the cell of a switchable capacitor array consists of two switches and two capacitors. The schematic of the cell is shown in Fig. 2. Assuming the switch is ideal, the capacitance of the capacitor array is given by

$$C_{array} = \frac{D_0 C}{2} + D_1 C + 2D_2 C + 4D_3 C + \dots + 2^{n-1} D_n C \quad (2)$$

where, $D_0, D_1, D_2, D_3, \dots$ and D_n are the controlled words of the switch with values of 1 or 0.

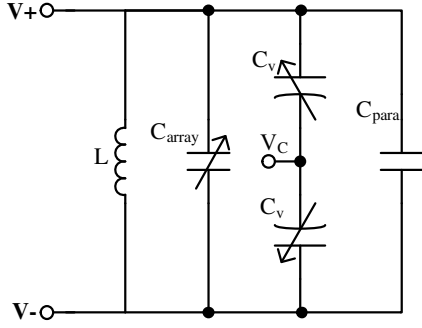


Figure 1: Equivalent circuit of the LC tank.

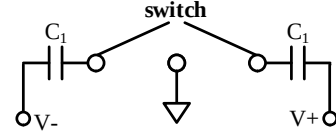


Figure 2: Schematic of the cell of switchable capacitor array.

The capacitance of the varactors depends on the value of V_c . Thus, the gain of proposed VCO is given:

$$K_{VCO} = \frac{\partial f_{osc}}{\partial V_c} = - \frac{1}{4\pi\sqrt{L} \left(\frac{C_v}{2} + C_{array} + C_{para} \right)^{1.5}} \frac{\partial C_v}{\partial V_c} \quad (3)$$

The tuning range (TR) of the proposed oscillation is given as:

$$TR = 2 \frac{\sqrt{\frac{C_{v,max}}{2} + C_{array,max} + C_{para}} - \sqrt{\frac{C_{v,min}}{2} + C_{para}}}{\sqrt{\frac{C_{v,max}}{2} + C_{array,max} + C_{para}} + \sqrt{\frac{C_{v,min}}{2} + C_{para}}} \quad (4)$$

The tuning range is determined by the capacitance ratio of the MOS varactors and the parallel switchable capacitor bank. In practice, the influence of the switch is important and shouldn't be neglected. The switch can be equivalent to a resistance R_{on} . The Equation (2) is changed and the equivalent admittance of the capacitor array is written as:

$$Y_{array} = \left(\frac{D_0}{2} + D_1 + 2D_2 + \dots + 2^{n-1}D_n \right) \cdot \left(\frac{j\omega_o C_1}{1 + (\omega_o C_1 R_{on})^2} + \frac{(\omega_o C_1)^2 R_{on}}{1 + (\omega_o C_1 R_{on})^2} \right) \quad (5)$$

Thus, the practical capacitance of the capacitor array is given by

$$C_{Parray} = \left(\frac{D_0}{2} + D_1 + 2D_2 + \dots + 2^{n-1}D_n \right) \frac{C_1}{1 + (\omega_o C R_{on})^2} \quad (6)$$

According to above, the conclusion could be drawn that the practical tuning range is smaller than Equation (4). Furthermore, maximum oscillation frequency is determined by inductor and varactors in LC tank and the extension of bandwidth is focus on the switchable capacitor array.

2.2. Analysis of Phase Noise

The phase noise of LC-tuned oscillator [11, 12] can be written as:

$$L(\Delta\omega) = 10 \log \left[\frac{kTR_{eff}(1+A)}{V_{max}^2/2} \left(\frac{\omega_0}{\Delta\omega} \right)^2 \right] \quad (7)$$

$$R_{eff} = R_L + R_C + \frac{1}{R_p(C\omega_o)^2} \quad (8)$$

Based on Equations (7) and (8), the phase noise of the LC-VCO depends on the equivalent resistance of LC tank and the amplitude of oscillation. The capacitor array of LC-VCO changes RC and C. Thus, Equation (8) can be written as:

$$R_{eff} = R_L + \frac{1}{\left(R_p \parallel R_{Parray} \parallel \frac{1 + (\omega_o C R_C)^2}{(\omega_o C)^2 R_C} \right) \left[\left(\frac{\omega_o C}{1 + (\omega_o C R_C)^2} + C_{Parray} \right) \omega_o \right]^2} \quad (9)$$

$$R_{Parray} = \frac{1 + (\omega_o C R_{on})^2}{\left(\frac{D_0}{2} + D_1 + 2D_2 + \dots + 2^{n-1}D_n \right) (\omega_o C)^2 R_{on}} \quad (10)$$

From the Equations (9) and (10), the conclusion can be drawn the capacitor array degrades the phase noise of LC-VCO.

According to Abidi model [13], the $1/f^2$ phase noise can be written as:

$$L(\Delta\omega) = \frac{8FkTR}{V_0^2} \left(\frac{\omega_0}{2Q\Delta\omega} \right)^2 \quad (11)$$

$$F = 1 + \frac{4RI\gamma}{\pi V_0} + \frac{4}{9}g_m R\gamma \quad (12)$$

And the structure of the LC-VCO, without tail current source, has better phase noise performance.

On the other hand, substrate noise and power noise are important sources of phase noise. In order to restrain substrate noise and power noise, LC filter network is inserted between a cross-coupled transconductance circuit and power. The resonant frequency of two LC filter networks can be written as

$$f \approx 2f_o \quad (13)$$

where f_o is the average of LC-VCO oscillation frequency.

2.3. Circuit Design

Based on the above analysis, the structure of the proposed wideband low phase noise LC-VCO is a double cross-coupled transconductance structure without tail current source, which is usually preferred in low-power and low phase noise applications. It consists of 4 parts, including a double cross-coupled transconductance circuit, an LC tank, two LC filter networks, and two isolation circuits for output nodes. The loss of the LC tank is canceled by the double cross-coupled transconductance circuit through generating a negative resistance. The LC tank consists of a spiral inductor, two MOS varactors, and a parallel switchable capacitor array. The parallel switchable capacitor array is a 4-bits coarse tuning element by changing the control codes and two MOS varactors are fine-tuning elements by changing the control voltages. It is shown in Fig. 3. And the cell of the parallel switchable capacitor array is shown in Fig. 2.

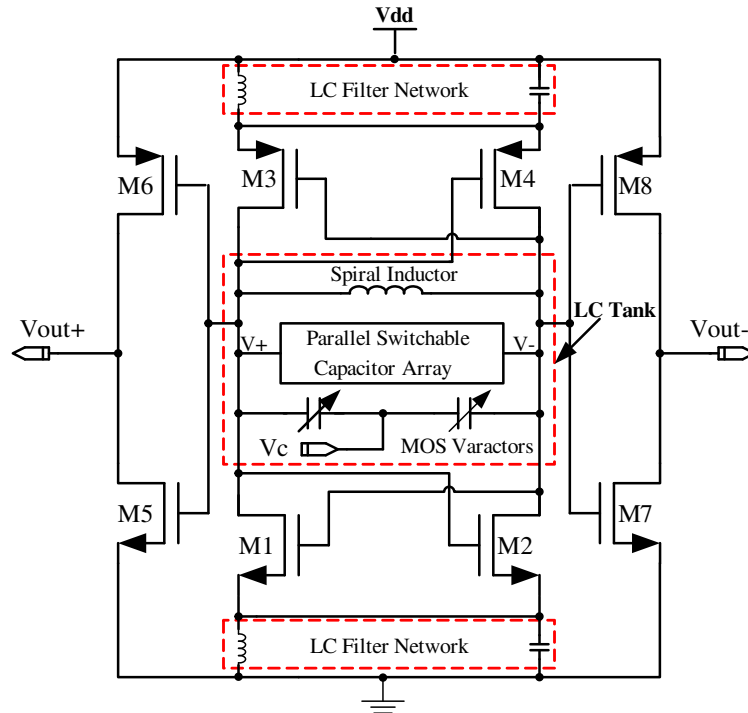


Figure 3: Schematic of the proposed VCO.

3. SIMULATION RESULTS

The wideband low-phase-noise VCO has been implemented in a SMIC's 0.18- μm RF CMOS technology. Fig. 4 shows the layout of the LC-VCO. The chip area is $650\text{ }\mu\text{m} \times 500\text{ }\mu\text{m}$, including the test buffer circuit and the pads.

The f - V curve of the proposed VCO is simulated as a function of the control codes of the parallel switchable capacitor bank. The simulated result is shown in Fig. 5. It decreases with the control codes changing from "0000" to "1111". This is consistent with Equations (1) and (6). And the tuning range is from 4.5 to 6.5 GHz and the average power consumption is 6.47 mW at 1.8 V power supply when the oscillating frequency is 6.5 GHz.

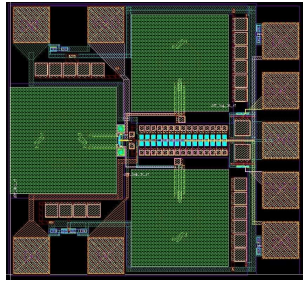


Figure 4: Layout of the proposed VCO.

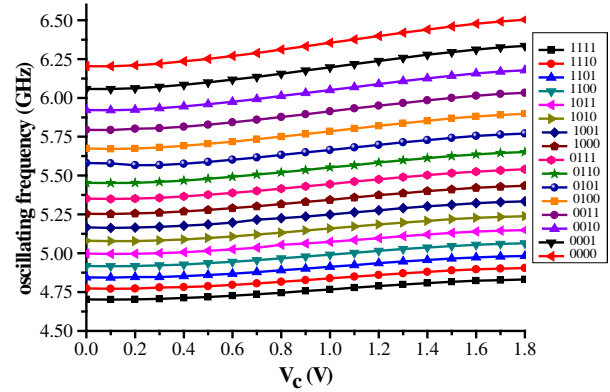


Figure 5: The simulated f - V curve of the proposed VCO.

To simulate the phase noise, the control voltage changes from 0 to 1.8 V with 0.1 V step and the control-code is from "0000" to "1111". In order to analyze and compare the phase noise in different controlled code and the different controlled voltage (V_c), the phase noise at 1 MHz offset is shown in the Fig. 6. The phase noise at 1 MHz offset is shown in the Fig. 7, which the controlled voltage (V_c) is 0 V. From the Figs. 6 and 7, it is seen that the different controlled code could lead to different phase noise. It is accordance with the Equations (7), (9) and (10).

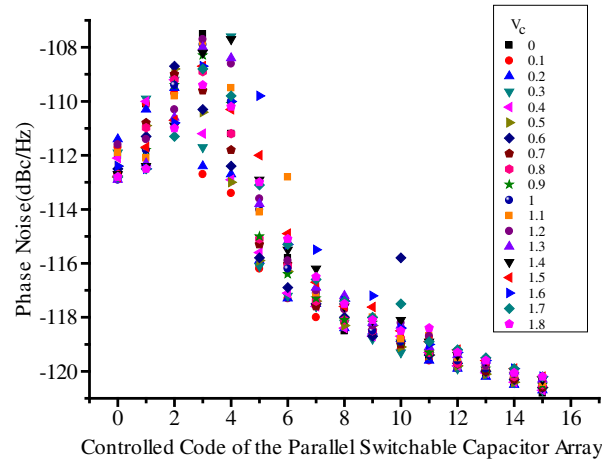


Figure 6: Simulated phase noise of the proposed VCO at 1 MHz offset.

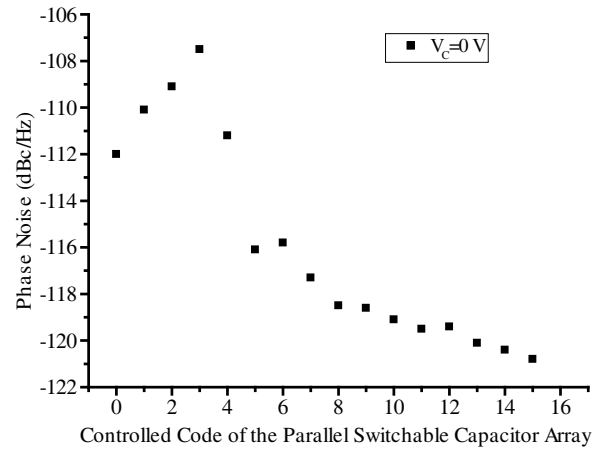


Figure 7: Simulated phase noise of the proposed VCO at 1 MHz offset.

4. CONCLUSION

The influence of the capacitor array is analyzed on tuning range and phase noise in LC-VCO. According to the analysis results, the wide band LC VCO with a low phase noise and low power consumption is designed. The simulated results show the tuning range of the proposed VCO is 36.4%. The simulating phase noise is -112.8 dBc/Hz at 1 MHz offset from the 6.5 GHz carrier.

The maximum average power consumption of the core part is 6.47 mW at 1.8 V power supply. On the other hand, the simulated results are in agreement with theories analysis.

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