A New Design of High-speed Decimal Direct Digital Frequency Synthesizer

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Abstract— The conventional direct digital frequency synthesizer (DDS) adopts a binary algorithm which limits the output frequency resolution in some applications and cannot switch frequency and phase quickly. To solve the problem, high-speed decimal DDS was proposed to improve the conventional DDS algorithm by using decimal and binary mixed algorithm and pipelined segments accumulator to realize the phase accumulation. In addition, the look-up-table (LUT) method is also adopted to achieve fast waveform output and it has shown high-speed and high-resolution performances. The new DDS is designed with VHDL language and its timing simulation results is also presented.

1. INTRODUCTION

Direct digital synthesizer (DDS) has been widely used in wireless communications due to its convenience and high frequency resolution. Although the resolution of the current design has been high, the binary operation phase accumulation restricts the minimum resolution of the DDS which is only 2^{-M}, where M is the number of accumulator bits, and this cannot meet a special output frequency requirement. In some applications, for example, in the terminal of very long baseline interferometry (VLBI) technology, more precise frequency signal is needed to adjust the received microwave signal. To satisfy this demand, the mixture of decimal and binary operation is used to enhance the DDS minimum frequency resolution to $2^{-M} \times 10^{-N}$, where M is the number of binary bits and N is the number of decimal bits.

The conventional DDS adopts a binary algorithm which limits the output frequency resolution in some cases and cannot switch the frequency and phase quickly. To solve this problem, the high-speed decimal DDS was proposed to replace the conventional DDS algorithm by using the mixture of decimal and binary algorithms and pipelined segment accumulator to realize the phase accumulation. It also uses a look-up table (LUT) to achieve a fast waveform output so that a high-speed and high-resolution performance can be achieved. We implement the new DDS design with VHDL language and its good performance has been demonstrated by simulations.

2. MAIN STRUCTURE OF DDS

. THE OVERALL STRUCTURE OF DDS

The basic block diagram of the DDS is shown in Figure 1. It consists of phase accumulator, waveform memory, D/A converter (DAC), and low pass filter (LPF). Here, the first three parts constitute a NC frequency synthesizer. Phase accumulator is the core part of DDS, and it begins to accumulate based on the phase offset and uses the frequency control word as a step. Once the output of accumulator overflows, it completes a cycle. Here the frequency control word and phase offset are set as the DDS input. The accumulator output in one cycle represents the phase of sinusoidal signal. Firstly, we divide the sinusoidal signal into M parts and store them in a ROM after quantification. Secondly, we use the look-up-table (LUT) method for the phase accumulator output data to output a corresponding amplitude data, and then obtain the corresponding step waveform through D/A converter. Finally, we use a low-pass filter to smoothen the step waveform and output a continuous sine wave.

The expression of sinusoidal signal is given by the following equation:

$$S_{out} = A\sin(w \cdot t) = A\sin(2\pi \cdot f_{out} \cdot t) \tag{1}$$

When expressing this Equation in digital logic, we have to transform it into a discrete time of one CLK cycle and $\Delta\theta$ represents the increased angle value.

$$\Delta\theta = 2\pi \cdot f_{out} \cdot T_{\mathrm{CLK}} = \frac{2\pi \cdot f_{out}}{F_{\mathrm{CLK}}} \tag{2}$$

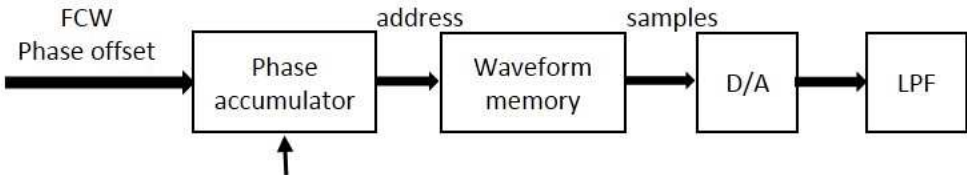


Figure 1: The basic block diagram of DDS.

To quantify the value of $\Delta\theta$, we divide 2π into $2^M \times 10^N$ parts and then express the phase increment in each CLK cycle in terms of $\beta_{\Delta\theta}$:

$$\beta_{\Delta\theta} = \frac{\Delta\theta}{2\pi} \times 2^M \times 10^N \tag{3}$$

Hence, the equation of sinusoidal signal in digital will be shown in the following equation in which θ_{K-1} represents the previous phase value:

$$S_{out} = A\sin\left(\theta_{K-1} + \Delta\theta\right) = A\sin\left[\frac{1}{2\pi \times 2^M \times 10^N}\left(\beta_{\theta_{K-1}} + \beta_{\Delta\theta}\right)\right] \tag{4}$$

Finally, we can get a conclusion based on Equation (1) to Equation (4), i.e., the phase increment $\beta_{\Delta\theta}$ (it is also called FCW) determines the signal output frequency. According to Equation (2) and Equation (3), the output frequency can be written as [1]:

$$f_{out} = \frac{K}{2^M \times 10^N} \cdot F_{\mathrm{CLK}} \tag{5}$$

. THE MIXED PHASE ACCUMULATOR

In DDS circuit, phase accumulator is a crucial part to determine the performance of DDS. Considering the internal structure of FPGA, we design a phase accumulator which not only meets the requirement of frequency resolution but also improves the system speed. Its structure is showed in

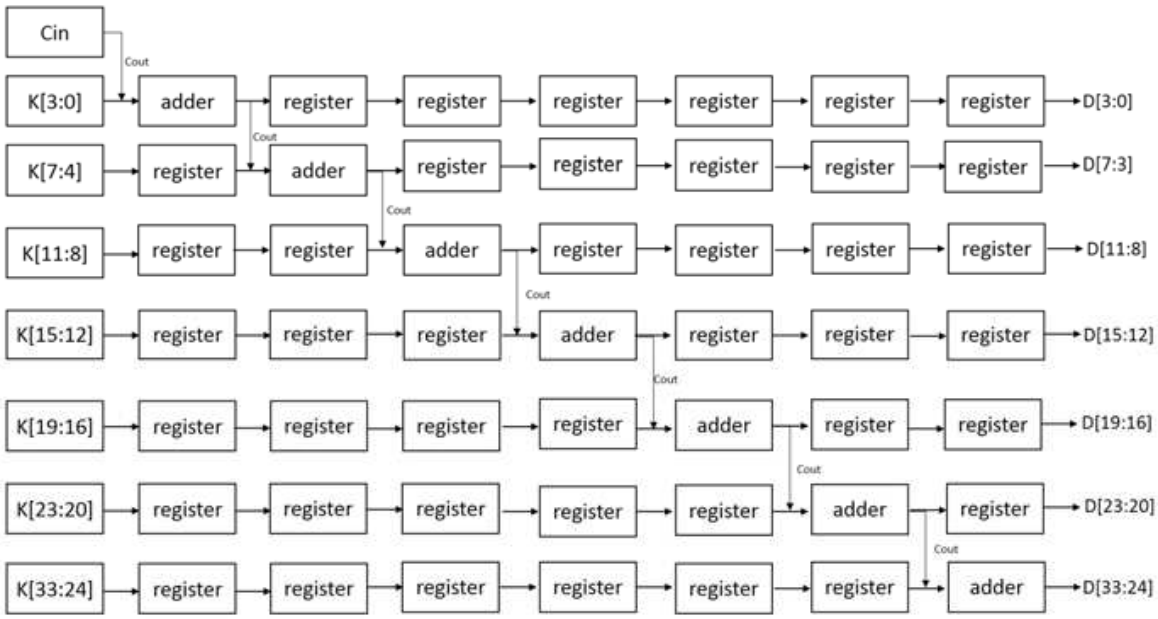


Figure 2: The structure of pipelined segment accumulator.

Figure 2. Here we design a 34-bits accumulator in which 10 bits are used for binary accumulation and 24 bits are used for decimal accumulation. The 24 bits are divided into 6 parts, and each part has 4 bits for transforming BCD-code operation. A pipelined-segments-accumulation algorithm is applied because if we use a very wide bits adder to constitute the accumulator directly. The adder delay will limit the accumulator's operating speed greatly [2]. Segment accumulator makes each part add their relevant bits in one stage, and then transmit the carry bit to next stage for further accumulation. Since each part operates in one stage and at the same time, the total delay just exists between the stages, the system speed will be improved greatly [3].

. PHASE TO AMPLITUDE CONVERSION

Phase-to-amplitude conversion is another important part of DDS circuit. In this system, we use the ROM look-up table to achieve the conversion. We divide the 2π section into several parts and quantify them by using phase accumulator outputs as addresses to look up their corresponding amplitude and finally output the amplitude. Due to the symmetry of sine wave, it is oddly symmetric in the sections of $[0 : \pi]$ and $[\pi : 2\pi]$ while it is evenly symmetric in the sections of $[0 : 0.5\pi]$, $[0.5\pi : \pi]$, $[\pi : 1.5\pi]$, and $[1.5\pi : 2\pi]$. Therefore, we can use one-fourth cycle of sine wave to get the whole cycle amplitude. We take the highest bit of phase accumulator outputs (MSB) to judge the positive or negative signal and use the second highest bit (MSB-1) to judge whether its address is reversed or not. The remaining bits are initial addresses which we use the phase to represent.

As shown in Figure 3, when MSB-1 is 0, meaning that the point is in two or four, the effective address is equal to phase. However, when MSB-1 is 1, which means that the point is in one or three, the effective address is 2^{MSB}-1-phase. When MSB is 0, it means that the amplitude is positive and the other is negative.

MSB	MSB-1	quadrant	Positive /negative	Address direction
0	0	One	+	normal
0	1	two	+	reverse
1	0	three	_	normal
1	1	four	_	reverse

Figure 3: Phase-to-amplitude conversion.

3. DESIGN EXAMPLE AND SIMULATION RESULTS

We design a DDS whose system clock (F_{CLK}) is 512 MHz and output value is 14 bits. We use 34-bits phase accumulator to ensure that the frequency resolution is sufficient and phase accumulator is of a 7-stage pipeline structure. The first part uses 10 bits to accumulate and the remaining 6 parts use 4 bits for each (BCD code) to accumulate. The phase-to-amplitude conversion is 14 bits and the last 20 bits of phase accumulator output are cut down. We set the input data pinc = "0000110000"&X"000000" and poff = "0011000000"&X"111111", then its ISim simulation result is shown in Figure 4. Here, pinc is the frequency control word (FCW) and poff means the phase offset.

The output sine waveform in time domain is shown in Figure 5(a) and Figure 5(b) illustrates the output phase continuity. Figure 6(a) and Figure 6(b) depict the simulation output in frequency domain after an FFT transformation and the abscissa of the pulse in Figure 6(a) is the desired design frequency. We enlarge the figure in Figure 6(b) to have a clear view and it can be seen that the output value is 24 MHz. To verify the correctness of the simulation, we set pinc = "0000110000"&X"000000", which is 48×10^6 in decimal system based on Equation (5).

$$f_{out} = \frac{48 \times 10^6}{2^{10} \times 10^6} \times 512\,\mathrm{MHz} = 24\,\mathrm{MHz} \tag{6}$$

This result is mapped with Figure 6(b), demonstrating that this design is successful.

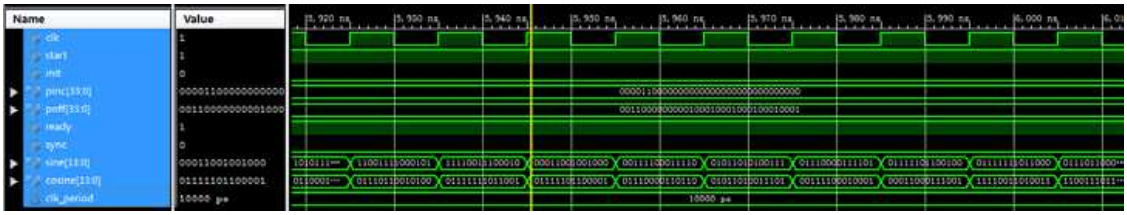
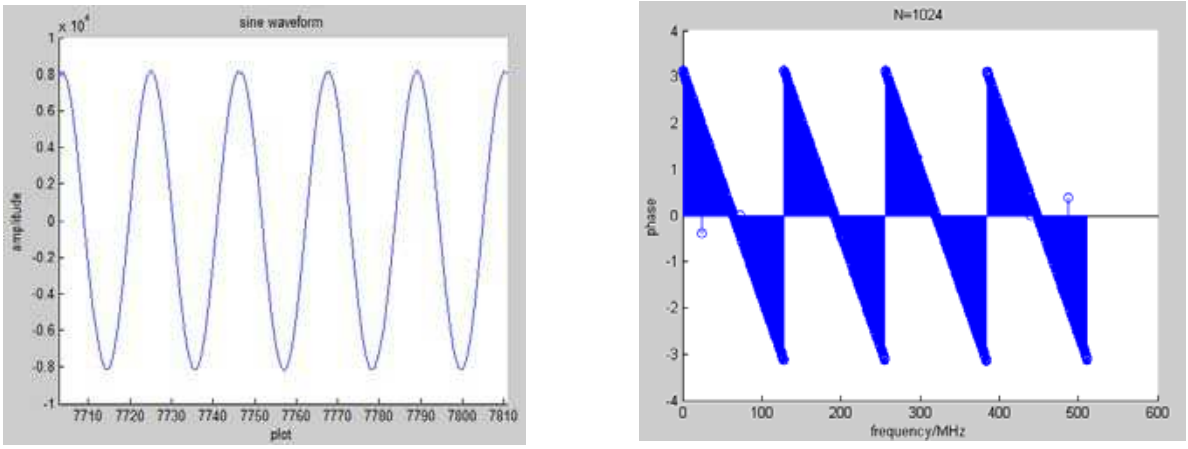
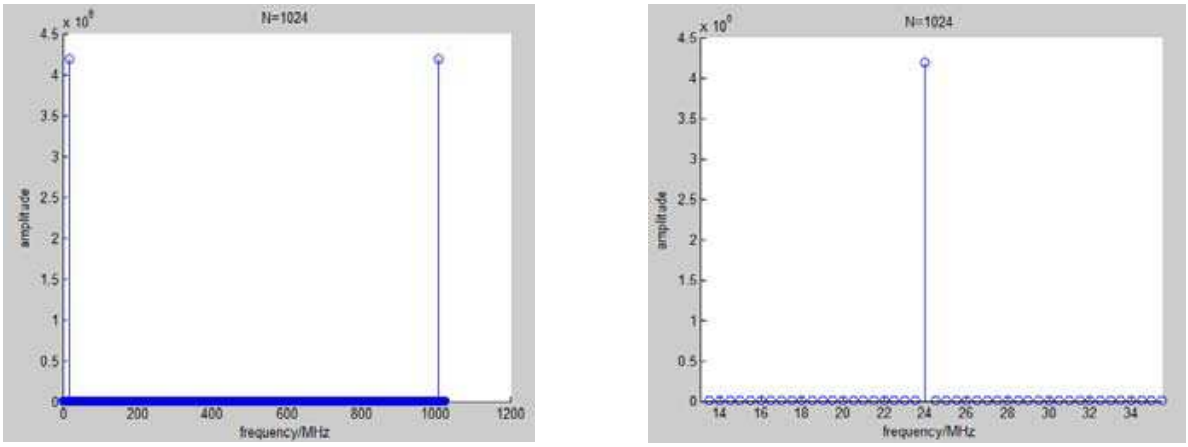


Figure 4: ISim simulation result.



(a) (b)

Figure 5: Output sine waveform and phase spectrum.



(a) (b)

Figure 6: Output sine frequency spectrum.

4. CONCLUSION

This paper introduces a mixed phase accumulator algorithm to meet frequency resolution and a pipelined-segments accumulation algorithm to improve the system's operating speed. Also, the simulation result is given to verify the realization of the idea. In the practical design, more details will be modified but the essential part will keep the same as in this paper.

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