High Speed Pipelined ADC Uses Loading-balanced Architecture

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Abstract— A 10-bit 200 MS/s Pipelined analog to digital converter (ADC) is realized using operational amplifier (op-amp) and capacitor sharing. A novel loading-balanced architecture is proposed to equal the capacitor load of the two adjacent stages which sharing one amplifier and reduce the load capacitor. Low power consumption is achieved by using loading-balanced architecture. The ADC is implemented in TSMC 0.18 µm 1P6M CMOS process. The supply voltage is 1.8 V. The simulation results show 57.7 dB SNDR and 61.13 dB SFDR with a 98 MHz input operating at a 200 MS/s sampling rate. The area is 1.2 mm × 1.2 mm.

1. INTRODUCTION

Applications such as wireless sensor networks, image recognition and medical instrumentation require high-speed high-resolution and low power consumption analog to digital converters (ADCs). Pipelined ADC has been widely used in these fields because it achieves a good compromise between speed, accuracy and power consumption. Meanwhile many circuit techniques such as sample-and-hold Amplifier (SHA)-less front end [1], op-amp sharing [2], capacitor sharing [3] and scaling down capacitor values through the pipeline [4] has been developed to reduce the power consumption.

In this work, a prototype of 10 bit 200 MS/s pipelined ADC with loading-balanced architecture is developed, Fig. 1 is the architecture of the ADC. The circuit consists of eight 1.5 bit/stage and a 2 bit back end flash ADC. It uses one op-amp less than the traditional ADC for using SHA-less architecture. the number of op-amp is reduced from 8 to 4 for op-amp sharing technique is used, the load capacitor of the first stage is reduced equal to the second stage for capacitor sharing technique, the non-standard inter-stage gain makes the feedback factor of the first stage increased equal to the second stage. So the load of op-amp shared by the first two stages is balanced. The capacitor load and feedback factor of the third and fourth stage are the same. The fifth to eight stage is the same as the third and fourth stage. From the system view, all the loads of the OTAs shared are balanced. The design power optimized.

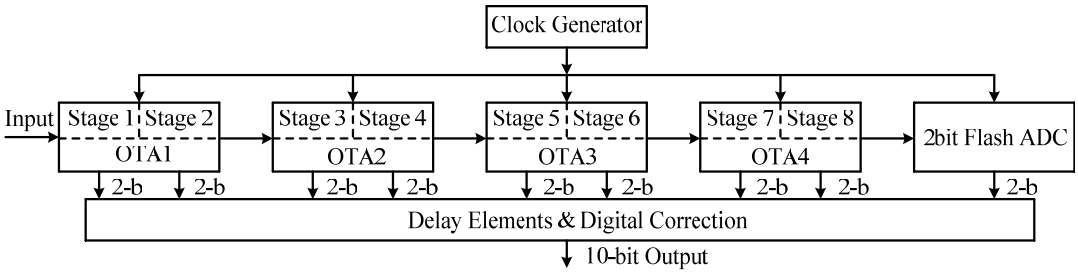

Figure 1: Architecture of the 12 bit loading-balance Pipelined ADC.

2. CIRCUIT DESIGN

2.1. The First and Second Stage with Loading-balanced Architecture

Figure 2 is the architecture of the first and second stage (the first unit), in order to lower the power consumption, noise contribution and reduce the die area. The loading-balanced pipelined ADC removes the first-end SHA, the input signal is sampled by the bootstrapped switch in directly. The ADC scaling down the capacitor value through the pipeline by the factor of 0.5, so when the first stage is settling in closed loop, the load capacitor is lager then the second stage. The shared op-amp is designed in accordance with the requirement of the first stage. So when the second stage is settling, a part of power will be wasted. The loading-balanced pipelined ADC using capacitor

sharing technique and non-standard inter-stage gain scaling down the load to the same with the second stage in settling, realizes the load balance between the two stages.

Figure 3 is the architecture of the first unit during four different phases. The Op-amp has two input pairs and works alternately to cancel the memory effect. The two pairs of the capacitors are working alternately controlled by the four non-overlapping clock phases which is shown in Figure 4. During the clock phase Φ_1, the schematic of the first unit shown in Figure 3(a), the first stage is sampling the input signal, the second stage is settling in closed-loop. The lower input pair of the op-amp and the top pair of the capacitors are resettling, removing the residual charge. During the clock phase Φ_2, the schematic of the first unit shown in Figure 3(b), the first stage is settling in closed-loop and producing the residue which is stored on the top pair of capacitors, the top input pair of the op-amp and the lower pair of the capacitors are resettling. During the clock phase Φ_3, the schematic of the first unit shown in Figure 3(c), the first stage of the unit is sampling the input signal, and the second stage is settling, the lower input pair of the op-amp and the lower pair of capacitors are resettling. Produce the residue which is utilized by the third stage. During the clock phase Φ_4, the schematic of the first unit shown in Figure 3(d), the second stage is settling in closed-loop and producing the residue which is stored on the lower pair of capacitors, the top input

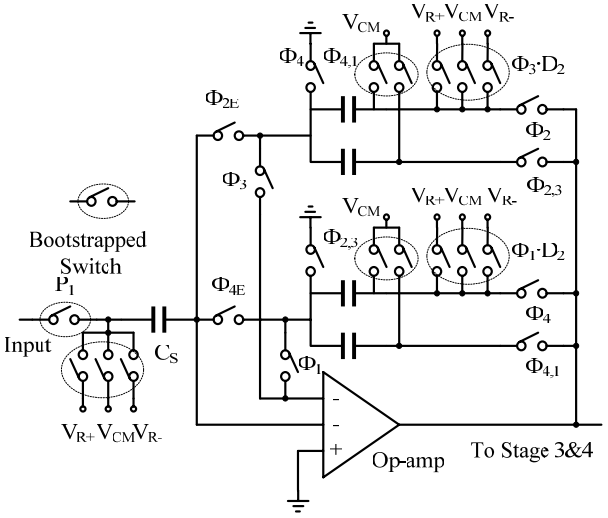

Figure 2: Schematic of the first unit.

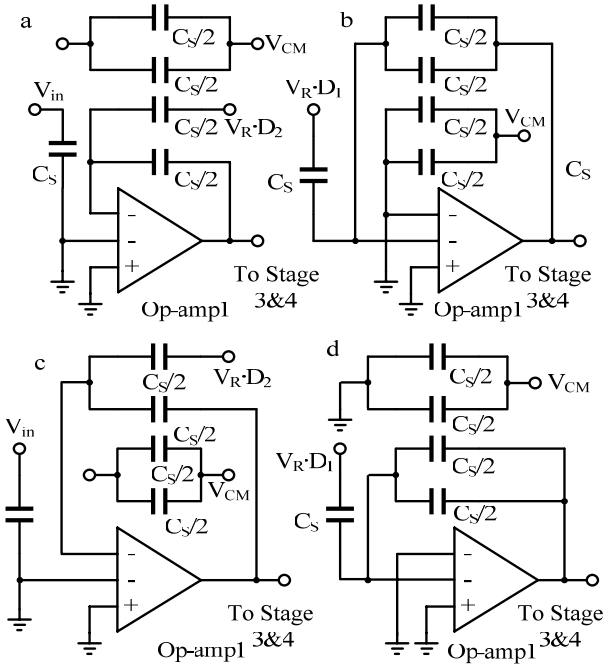

Figure 3: Architecture of the first unit in four phases.

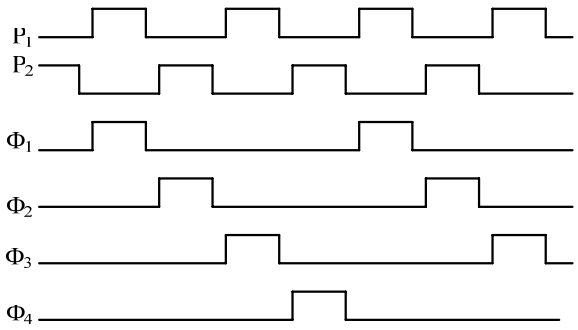

Figure 4: The clock signal used in Pipelined ADC.

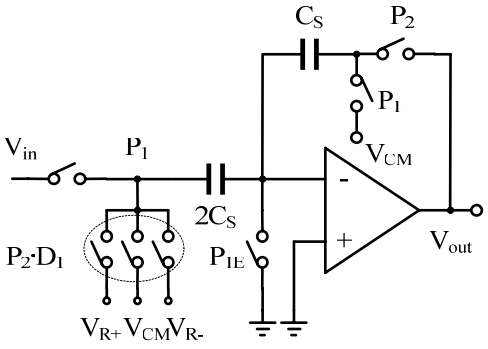

Figure 5: The conventional 1.5 bit/stage architecture.

pair of the op-amp and the top pair of the capacitors are resettling.

2.2. The Non-standard Inter-stage Gain Architecture

In conventional 1.5 bit/stage architecture, the gain of the multiplying digital-to-analog converter (MDAC) is two, the feedback factor is 0.5, all the stages have the same input and output range, the value is $\pm V_R$. Because the first stage using SHA-Less architecture, mismatch between sampling paths of comparator and MDAC leads to aperture error [5]. The conventional MDAC shown in Fig. 5 remove the mismatch successfully, but the feedback factor is 1/3, it wastes a part of power, and the load compactor value between the first and second stage are different.

In this design, a novel non-standard inter-stage gain architecture is proposed, the architecture is shown in Fig. 6, it reduces the value of sample compactor from $2C_S$ to C_S. The gain of the MDAC reduces from 2 to 1 [6], then the input range increase to $\pm 2V_R$, and the feedback factor increases to 0.5, the threshold of the comparators in first Sub-ADC increase from $\pm 1/4V_R$ to $\pm 1/2V_R$. The transfer functions of the two MDACs are shown in Fig. 7. The equivalent load capacitor values of the first and stage are the same, the value is $Cs/2$, it realizes the loading balanced and reduced the consumption.

The third and fourth stage (the second unit) use conventional 1.5 bit/stage which is shown in Fig. 8. The shared Op-amp has two input pairs to cancel the memory effect [7]. This unit uses capacitor sharing technique to realize the loading balance between the two stages, the sample capacitors of the second unit scaling down to $Cs/8$, the total value of the third stage is $Cs/4$. The sample capacitors of the fourth stage are not scale down further. Because the value of sample capacitor is near to parasitic capacitor. The load capacitor is not scales down substantially.

But the feedback factor will reduced evidently. So the value of the sample capacitors between the third and fourth stage is same. The five to eight stages are same to the third and fourth stage, so the value of the equivalent load capacitors is same.

3. SIMULATION RESULTS

The ADC is designed in TSMC 0.18 µm 1P6M CMOS process. The layout of the ADC is shown in Fig. 9. The Section A is the first and second stage, Section B is the third and fourth stage,

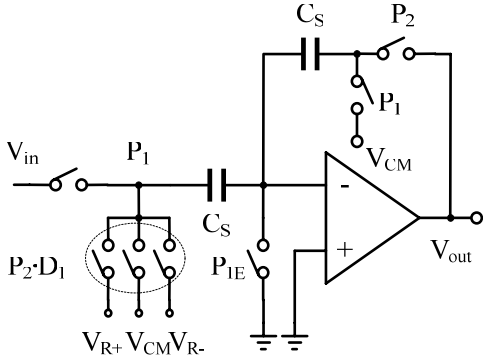

Figure 6: The non-standard inter-stage gain architecture.

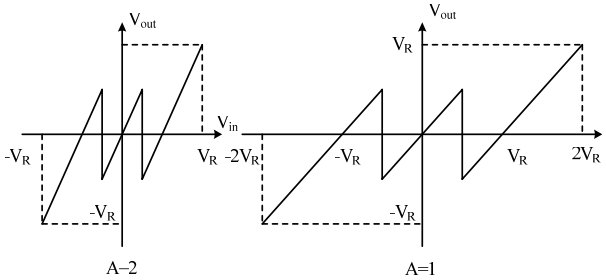

Figure 7: The two transfer functions.

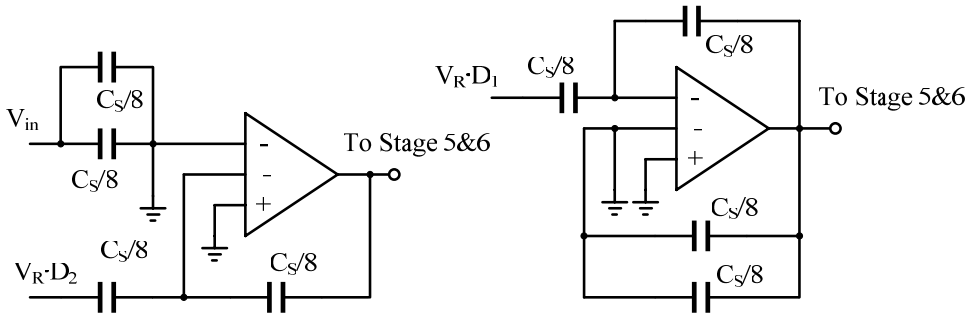

Figure 8: The conventional 1.5 bit/stage architecture.

Section C is the five and six stage, Section D is the seven and eight stage, Section E is the digital logical circuit, Section F is the output buffer circuit. The area is 1.2 mm × 1.2 mm. The ADC operates under supply of 1.8 V. The single-end input swing is 1.2 V. The simulation output FFT spectrum with 98.4 MHz input frequency at 200 MS/s is shown in Fig. 10, which exhibits SNDR of 57.68 dB and SFDR of 61.13 dB. Fig. 11 reveals the SNDR and SFDR of the ADC for an input frequency sweep at 200 MS/s.

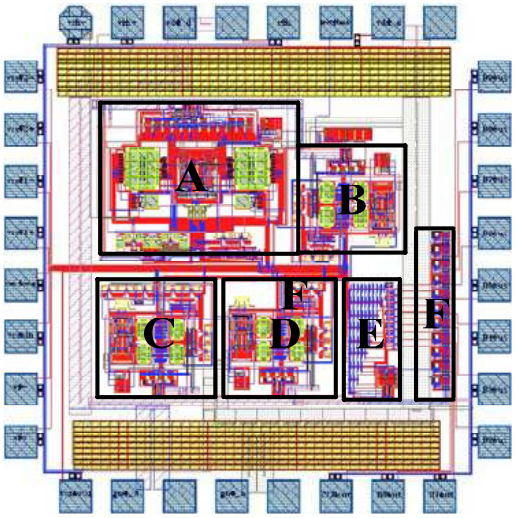

Figure 9: The layout of the ADC.

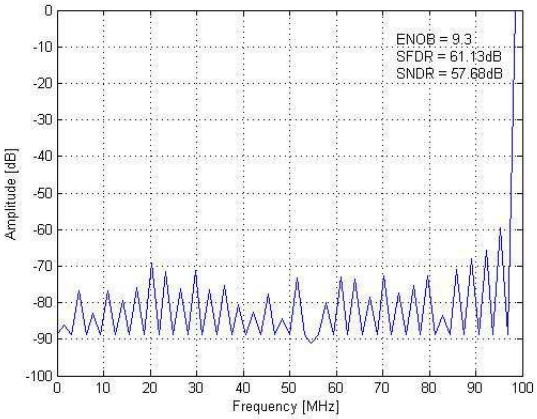

Figure 10: ADC output spectrum.

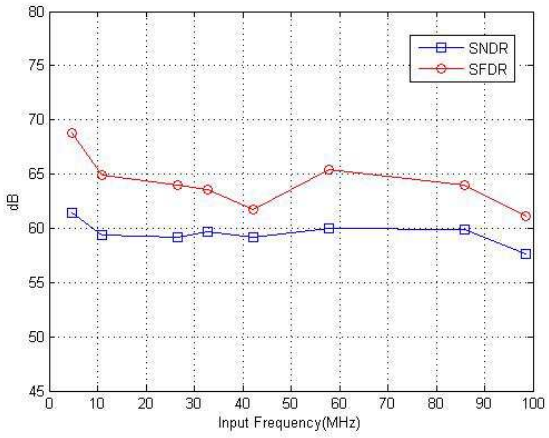

Figure 11: Dynamic performance versus input frequency.

4. CONCLUSION

This paper presents a 10 bit 200 MS/s pipelined ADC with 1.8 V supply. A novel loading-balanced architecture is proposed to equal the load capacitor of the two adjacent stages which sharing one amplifier. A non-standard inter-stage gain architecture is proposed to equate the load capacitor value between the first and second stage. reduce the load capacitor and power consumption. The third to eight stages are the same, so the equivalent load capacitors are the same, so the entire system realizes loading balance and reduces the power consumption. The method is verified by the experimental chip's simulation results, and showing SNDR of 57.68 dB and SFDR of 61.13 dB at 98.4 MHz input frequency, the power is 115 mW at 200 MHz sample frequency.

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