A Dual V-band Push-push VCO Using the 0.18 μm CMOS Process Technology

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Abstract— In this paper, a dual-band push-push voltage-controlled oscillator implemented in the 0.18-μm CMOS process for V-band applications is presented. By using a forth order resonance network composed of symmetric inductors and varactors and a push-push topology, the oscillation frequencies of the proposed circuit can be switched with only one control signal between two bands. And the second order harmonic is extracted from the central taps of inductors to achieve the frequencies of two V-band operations. The tuning ranges of the proposed voltage-controlled oscillator are from 67.78 to 69.42 GHz and from 52.2 to 54.7 GHz, respectively. The measured phase noise at 1 MHz frequency offset are −86.4 dBc/Hz and −90.5 dBc/Hz for 69.42 GHz and 54.7 GHz output frequencies, while the corresponding phase noises at 10 MHz frequency offset are −108.4 dBc/Hz and −112 dBc/Hz, respectively. The core circuit consumes a 12.96 mW dc power from a 1.8-V supply.

1. INTRODUCTION

Wireless communication systems operated in the millimeter-wave bands have been developed in recent studies [1–7]. In the transceiver front end, the voltage-controlled oscillator (VCO) is an essential building block of the frequency synthesizer which generates a local oscillator (LO) signal to perform modulation and demodulation functions Adopting the CMOS process technology to implement VCO designs is popular due to its low cost and high integration. V-band VCOs implemented by using the CMOS process technologies have also been proposed [1–4] successfully. However, these previous works were only designed for single band and they were not suitable for multiband applications [5]. Although the VCO proposed in [6] has two resonant modes by using the fourth order LC tank, it was designed at lower frequencies and not for V-band applications. Because of the limitation of the CMOS devices, it is a difficult task to design a dual-band VCO in the 0.18-μm CMOS process technology for V-band applications.

The purpose of this paper is to present a dual band VCO with a fourth order LC tank with the push-push topology that operates in the V band to overcome above limitation by utilizing the TSMC 0.18-μm CMOS process technology. This paper is organized as follows. In Section 2, circuit design of the proposed dual V-band push-push VCO is discussed. The measured results of the fabricated chip are shown in Section 3. And a short conclusion is given in Section 4.

2. CIRCUIT DESIGN

Figure 1 shows a simplified diagram of the RF frond end for a dual V-band receiver. Signals from the antennas are firstly fed in the band pass filters (BPFs) to filter out the out-of-band interferences. The desired signals from the BPFs are selected by a switch and the received RF signals are amplified by using a dual band low-noise amplifier (LNA). A wide band mixer named as 1st Mixer is used to convert the RF signals to the IF band by mixing with the V-band local oscillation (LO) signals. The dual V-band VCO is utilized to provide the required V-band LO signals in such a receiver.

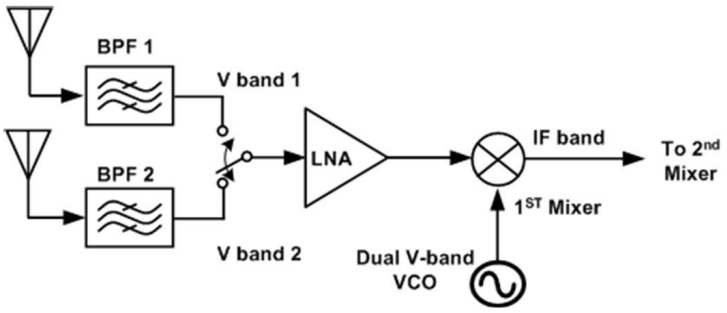

Figure 1: Simplified diagram of the RF frond end with a dual V-band receiver.

As indicated in the previous section, it is difficult to design a dual-band VCO for the V band applications by adopting the 0.18-μm CMOS process. One possible method to extend the operation frequency of a VCO is the push-push technique [3]. To generate the V-band LO signals for a dual V-band operation, the proposed VCO utilizes a fourth order LC tank with only one controlled voltage. Compared with using two VCOs for each band, the proposed circuit topology has the advantage on design and cost. Figure 2 shows the schematic of the proposed dual V-band VCO in which the tank formed by varactors C_{VAR1}, C_{VAR2}, inductors L_1, L_2, L_3, and parasitic capacitance (C_P; not shown explicitly in Figure 2) is for output frequency selections of the V band 1 and V band 2 via the controlled voltage V_C and a cross-coupled transistors pair (M_1–M_2) is used for compensating the losses of the tank including other parasitic effects. The current source (I_B) provides the required dc bias current for the VCO core. We design the proposed dual V-band VCO by deriving the impedance of the fourth order network. Due to the symmetry, the impedance of the half circuit of the fourth order LC tank neglecting losses in the tank can be derived as

$$Z(s) = \frac{s^3 L L_3' C_{\mathrm{VAR}} + s L_3'}{s^4 L L_3' C_{\mathrm{VAR}} C_P + s^2 (L C_{\mathrm{VAR}} + L_3' C_{\mathrm{VAR}} + L_3' C_P) + 1}, \tag{1}$$

where L and C_{VAR} represent the corresponding quantities with subscript 1 or 2, and L_3' indicates the single-end inductance of L_3 in the half circuit. The oscillation occurs if the denominator in (1) becomes 0 with $s = j2\pi f_{osc}$ which leads to two possible solutions expressed as

$$f_{osc} = \frac{1}{2\pi} \left(\frac{B \pm \sqrt{B^2 - 4A}}{2A} \right)^{\frac{1}{2}} \tag{2}$$

where $A = L L_3' C_{\mathrm{VAR}} C_P$ and $B = L C_{\mathrm{VAR}} + L_3' C_{\mathrm{VAR}} + L_3' C_P$.

Output oscillation signal with a second order harmonic ($2f_{osc}$) is extracted from the middle terminal of the center-tap inductors (L_2–L_3) connected commonly and an open-drain output buffer amplifier is adopted via buffer capacitance (C_B) for the chip measurements.

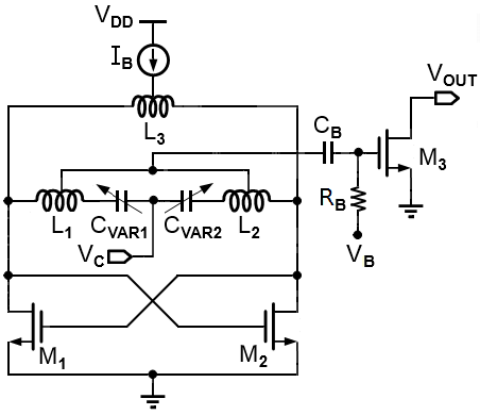

Figure 2: Schematic of the proposed VCO.

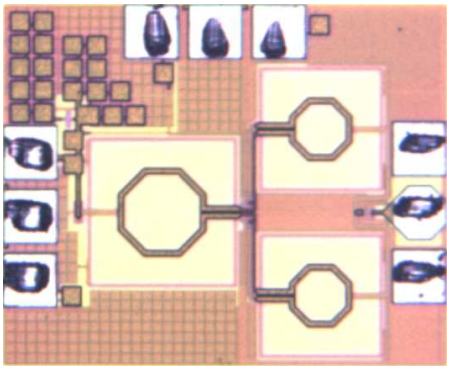

Figure 3: Micrograph of the proposed VCO.

3. MEASURED RESULTS

The proposed VCO is fabricated in the TSMC 0.18 μm CMOS process technology. The micrograph of the chip is as shown in Figure 3. And the chip area is $0.695 \times 0.565\,\mathrm{mm}^2$. The core circuit and the output buffer of the proposed VCO consume 12.96 mW and 8.1 mW dc power, respectively from a 1.8-V power supply. The cable loss was not calibrated in the following measured results.

Figures 4(a) and 4(b) show the measured output spectrums of the proposed VCO for V band 1 that is the lower band and V band 2 that is the upper band. Their output frequencies can be seen are 54.7 GHz with a measured power of −41.84 dBm without calibrating the 10 dB line loss and 69.42 GHz with a measured power of −47.22 dBm without calibrating 16 dB line loss, respectively. Figure 5(a) shows the measured phase noises of the proposed VCO for V band 1 and it reads −90.5 dBc/Hz and −112 dBc/Hz at 1 MHz and 10 MHz frequency offsets, respectively, under 54.7 GHz output frequency And Figure 5(b) shows the measured phase noises of the proposed

VCO for V band 2 and it reads −86.4 and −108.4 dBc/Hz at 1 MHz and 10 MHz frequency offsets, respectively under 69.42 GHz output frequency. Figures 6(a) and 6(b) show the measured tuning ranges of the proposed VCO for V band 1 and V band 2, respectively, and the tuning range for V band 1 is from 52.2 GHz to 54.7 GHz with the controlled voltage V_C swept from 1.1 V to 1.8 V while the tuning range for V band 2 is from 67.78 GHz to 69.42 GHz with the controlled voltage V_C swept from 0 V to 1 V.

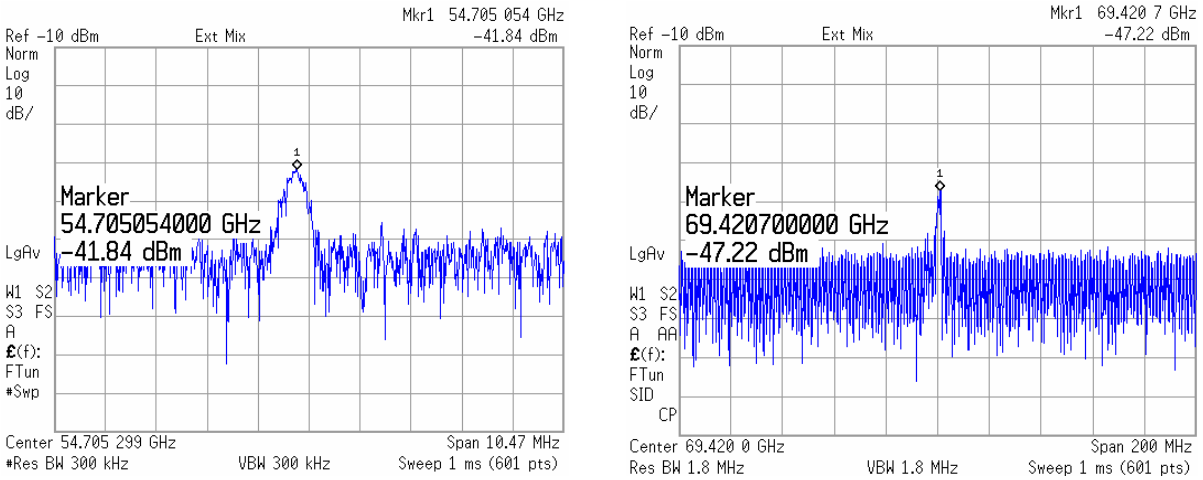

Figure 4: Measured output spectrums for (a) V band 1 and (b) V band 2.

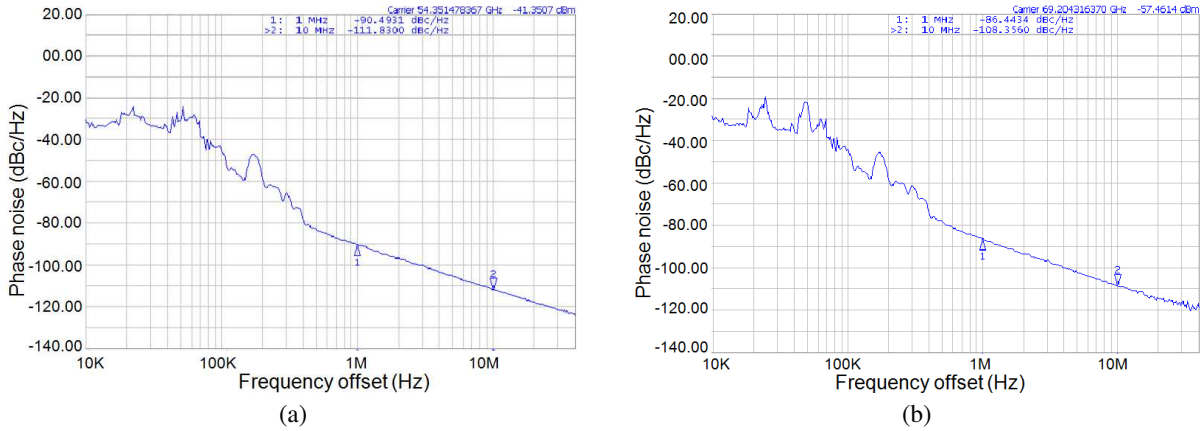

Figure 5: Measured phase noises for (a) V band 1 and (b) V band 2.

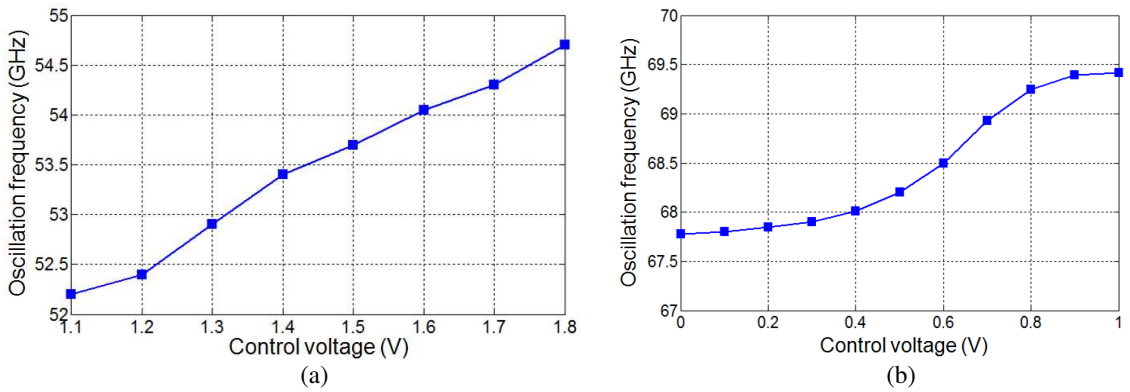

Figure 6: Measured output tuning ranges for (a) V band 1 and (b) V band 2.

4. CONCLUSIONS

In this paper, we have proposed a dual-band push-push VCO implemented in the TSMC 0.18-μm CMOS process for V-band applications. The proposed VCO adopts a fourth order resonant network to generate two oscillations for V band 1 and V band 2 switched by only one controlled voltage. The measured phase noises at 1 MHz frequency offset are −86.4 dBc/Hz and −90.5 dBc/Hz, respectively, around 68.5 and 53.3 GHz of the output frequencies. And the measured tuning ranges of the proposed VCO are 2.4% and 4.65% for the upper band and the lower band, respectively. The core circuit of the proposed VCO consumes a 12.96 mW dc power under a 1.8-V supply.

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REFERENCES

1. Shigematsu, H., T. Hirose, F. Brewer, and M. Rodwell, "Millimeter-wave CMOS circuit design," *IEEE Trans. Microw. Theory Tech.*, Vol. 53, No. 2, 472–477, 2005.
2. Hsieh, H. H. and L. H. Lu, "A V-band CMOS VCO with an admittance-transforming cross-coupled pair," *IEEE J. Solid-State Circuits*, Vol. 44, No. 6, 1689–1696, 2009.
3. Chiu, H. C. and C. P. Kao, "A wide-tuning-range 69 GHz push-push VCO using 0.18 μm CMOS technology," *IEEE Microw. Wireless Compon. Lett.*, Vol. 20, No. 2, 97–99, 2010.
4. Li, L., P. Reynaert, and M. Steyaert, "A 60 GHz CMOS VCO using capacitance-splitting and gate-drain impedance-balancing technique," *IEEE Trans. Microw. Theory Tech.*, Vol. 59, No. 2, 406-413, 2011.
5. Li, Z. and K. K. O, "A low-phase-noise and low-power multiband CMOS voltage-controlled oscillator," *IEEE J. Solid-State Circuits*, Vol. 40, No. 6, 1296–1302, 2005.
6. Jang, S. L., Y. K. Wu, C. C. Liu, and J. F. Huang, "A dual-band CMOS voltage-controlled oscillator implemented with dual-resonance LC tank," *IEEE Microw. Wireless Compon. Lett.*, Vol. 19, No. 12, 816–818, 2009.
7. Yi, X., C. C. Boon, J. Sun, N. Huang, and W. M. Lim, "A low phase noise 24/77 GHz dual-band sub-sampling PLL for automotive radar applications in 65 nm CMOS technology," *IEEE Asian Solid-State Circuits Conference (A-SSCC)*, 417–420, Nov. 11–13, 2013.