A 30-GHz Low Phase Noise LC VCO and Frequency Divider in 90-nm CMOS Technology

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Abstract— This paper presents the design of a 30-GHz low phase noise LC-tank voltage control oscillator (VCO) and a high speed frequency divided-by-two module in a 90-nm CMOS technology. A single cross-coupled PMOS transistor pair with drain resistors is adopted to suppress the flicker noise up-conversion. To improve the linearity, two sets of varators with different DC biasing are implemented. The simulated tuning range of the VCO covers from 28.7 to 32.4 GHz in four tuning curves. The simulated output phase noise at offsets of 10 kHz, 100 kHz and 1 MHz are −50, −78, and −104 dBc/Hz, respectively. The power consumption of the VCO is 9 mW under a 1.2-V power supply. A current mode logic (CML) divided-by-two module is designed to operate at 28 to 40 GHz. The divider core draws 3.3 mA from a 1.2-V supply.

1. INTRODUCTION

In the fast-booming wireless communication market, more and more millimeter wave frequency bands are up-coming and pose the challenges of microwave CMOS chips. In China, the 59 ∼ 64-GHz frequency band has been assigned for these applications, and recently a 45-GHz band of Q-band has been developed to support both long-range and short range high data rate wireless communications.

In a typical double-conversion low intermediate frequency receiver architecture for the 45-GHz applications, considering a first intermediate frequency (IF) of 15 GHz and a low second intermediate frequency, two local oscillator (LO) signals can be generated by a 30-GHz LC voltage control oscillator (LC-VCO) and its divided-by-two frequency divider. This paper presents the design of a 30-GHz narrow-band VCO and its high speed divider using a standard 90-nm CMOS process. Two drain resistors are adopted in the VCO to suppress the flicker noise up-conversion.

The paper is organized as follows: Section 1 is the introduction of the recent development of microwave wireless communications. Section 2 presents the VCO architecture and the phase noise enhanced technology. The current mode logic (CML) based divider structure and its operation are described in Section 3. Simulation results and conclusion are provided in Sections 4 and 5, along with a comparison of the presented work with other recent works.

2. VCO DESIGN

The schematic of the proposed VCO is shown in Fig. 1(a). It is an LC difference VCO with single NMOS cross-coupled devices. Two resistors R_D are inserted in series to the drain of the cross-coupled MOSFETs.

In practice, other suppression techniques have been used such as adopting a resonant network at the drain of the current source or inserting resistors in series to cross-coupled transistor sources. The former solution requires an LC resonant filter tuned to the $2f_0$ where f_0 is the oscillation frequency of the VCO. In wide band applications, a tuning mechanism needs to be added. The second solution reduces the harmonic generation at expenses of excess gain and start-up margin [1].

By inserting the resistors at the drain of the transistors, the excess gain of a single PMOS can be expressed as

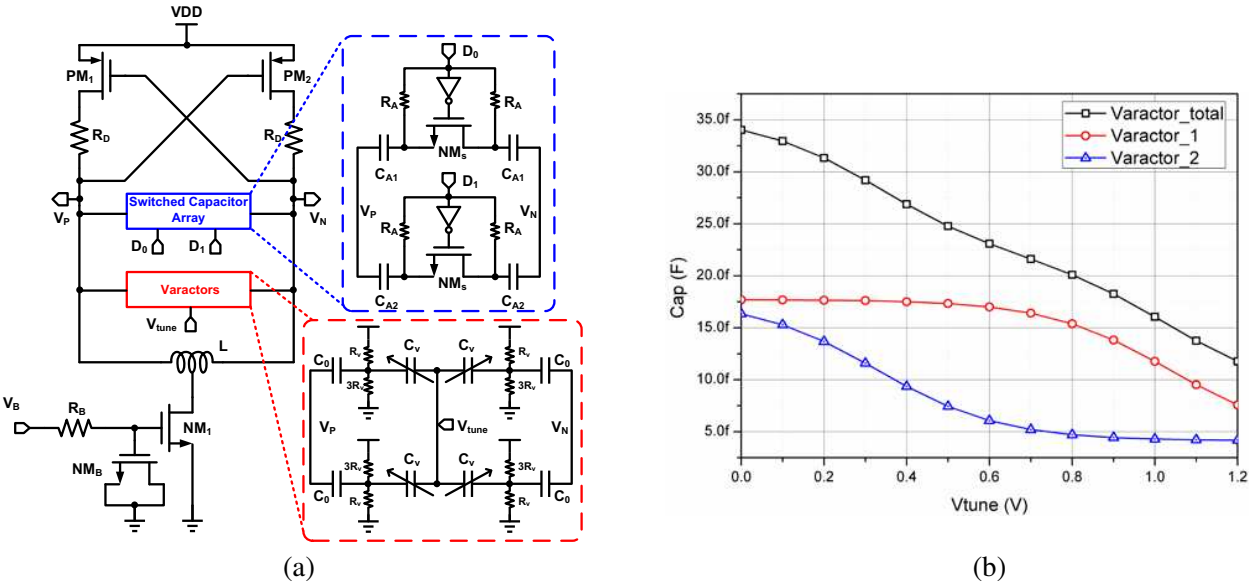
$$G_X \approx g_{mp} R_D, \tag{1}$$

where g_{mp} is the transconductance of the PMOS transistor. The added delay causes by R_D can be estimated by

$$\tau_D \approx \omega_0 R_D C_D, \tag{2}$$

where C_D is the parallel capacitor at the drain of $PM_{1,2}$. The ideal suppression condition could be achieved when the following formula is met [2].

$$\left[\frac{G_X - 1}{4Q} - \omega_0 R_D C_D\right] + \left[\frac{(G_X - 1)^2}{8Q} - \frac{1}{2}\omega_0 R_D C_D\right] = 0 \tag{3}$$



(a) (b)

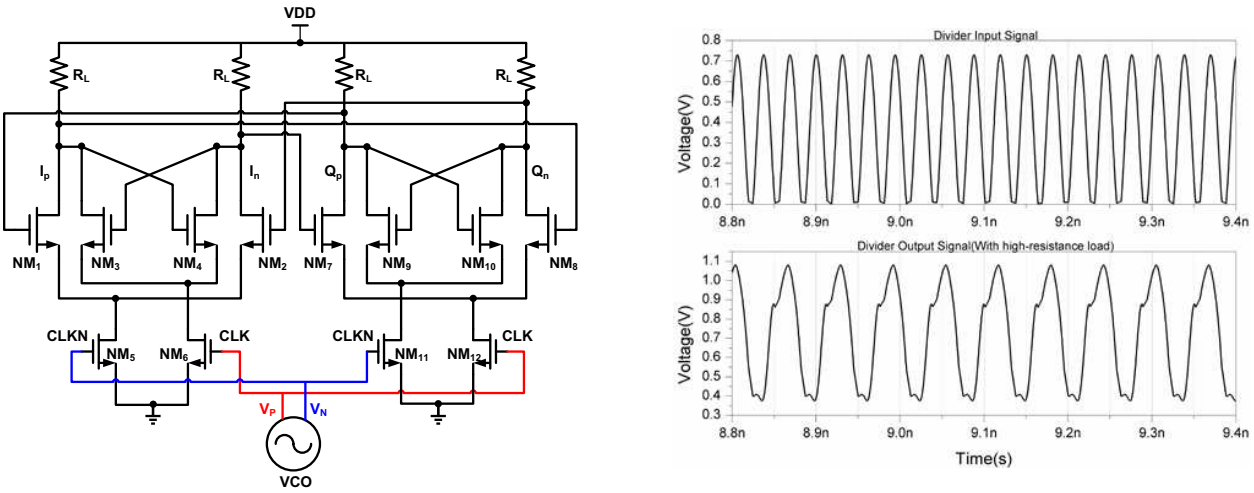
Figure 1: (a) LC-VCO topology with drain resistors. (b) Simulated varactor C-V curves.

Thus the optimum value of the drain resistor to suppress the flicker noise up-conversion is

$$R_D \approx \frac{G_X^2 - 1}{12Q\omega_0 C_D} \tag{4}$$

For the designed VCO, the quality factor of the inductor at 30 GHz can be as high as 40, and the g_m is designed to be large to ensure the start-up margin. To achieve a required output amplitude of the oscillator, a large current is usually needed. While a large resistance results a large voltage drop across the resistor, the output power of the VCO will be reduced, so the resistor size should be chosen wisely. G_X is usually set between 2 and 4 also to ensure the start-up.

Two varactor units are used as the voltage controlled module. Because of the poor linearity of a single varactor, two units are biased in different DC operating points. The simulated C-V curve is shown in Fig. 1(b). The VCO has a tuning range of about 3.7 GHz from 28.7 to 32.4 GHz, which covers the desired frequency bands. Based on the parameter we calculated above, the VCO gain is about 1 GHz/V on average.



(a) (b)

Figure 2: (a) The schematic of divided-by-2 CML divider. (b) Simulated transient waves of the divider.

3. DIVIDER DESIGN

In order to generate quadrature LO signals, two identical CML latches are used to build up a master-slave configuration. The input clock signals are coming from the 30-GHz LC-VCO, which is directly coupled to the clock transistors' gate. Thus, the gate capacitors should be considered while designing the VCO. In order to operate under a 1.2-V power supply voltage, the tail current sources have been removed. The schematic of the proposed divider is shown in Fig. 2(a).

The self-oscillation frequency has been set to 32 GHz. In each latch, the most of the current should be made flow through the sample pairs and the hold pairs only need about 1/3 of the total current. The sample pairs and hold pairs serve as analog mixers in each latch. Two latches, notified as latch I and Q, connected in a negative feedback loop. The whole CML divider can be seen as a ring oscillator. According to Barkhausen criterion, the locking range of the divider is restricted by the loop phase and loop gain. To reach the maximum locking range, the condition $g_{mh} \cdot R_L = 1$ should be satisfied, where g_{mh} is the transconductance of the hold pair. The simulated transient waves are shown in Fig. 2(b).

4. SIMULATION RESULTS

The 30-GHz LC-VCO and divided-by-2 CML frequency divider are designed in a standard 90-nm CMOS technology. The layout of the proposed schematics is shown in Fig. 3 with an area of

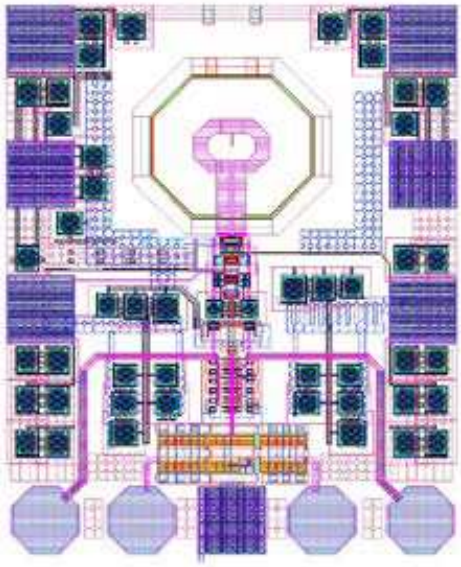


Figure 3: Layout of the proposed VCO and divider.

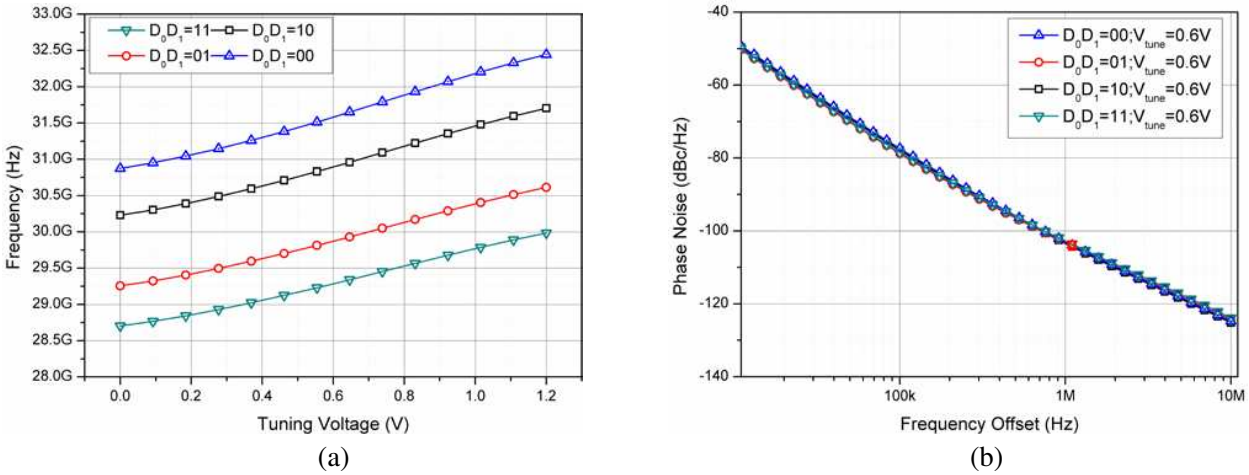


Figure 4: (a) Simulated tuning curves of the VCO. (b) Simulated phase noise of the VCO.

Table 1: Summary of the performance and comparison with SOA.

Ref.	Frequency Range (GHz)	Power Supply (V)	Phase Noise (dBc/Hz)	Power Consumption (mW)	Technology
3	53.2–58.4	0.7/0.43	−90.08, @1 MHz	1.2	90 nm CMOS
4	12.72–12.93	1.2	−105.25, @1 MHz	3	90 nm CMOS
5	38–43	1.2	−86.46, @1 MHz	5.9	90 nm CMOS
6	55.5–61.5	1	−90, @1 MHz	3.9	0.13 µm CMOS
This work	**28.7–32.4**	**1.2**	**-50, @10 kHz -78, @100 kHz -104, @MHz**	**9**	**90 nm CMOS**

$609 \times 497\,\mu m^2$. The VCO operates at the supply voltage of 1.2 V and draws an average current of 7.5 mA, and the divider consumes an average current of 3.3 mA under the same supply voltage.

The simulated tuning curves are plotted in Fig. 4(a). The simulated tuning range of the VCO covers from 28.7 to 32.4 GHz in four tuning curves. By adding the drain resistors, the phase noise of the VCO has a promotion in the closed-in frequency offsets. Fig. 4(b) shows that the output phase noise at an offset of 10 kHz, 100 kHz, and 1 MHz is −50, −78, and −104 dBc/Hz, respectively. Furthermore, different phase noise in different working frequency shows a small variation due to the delay brought in by the drain resistor.

5. CONCLUSION

In this work, a low phase noise 30-GHz LC-VCO with drain resistors and its divided-by-2 module are designed in a standard 90-nm technology. By adopting the drain resistors, the phase noise of the VCO has promoted phase noise performance at its closed-in frequency offsets. The CML divider operates within the frequency range of 22 to 40 GHz and generate quadrature LO signals.

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