10 bit 100 MS/s SAR ADC with Reduced Loop Delay

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Abstract— A 10 bit 100 MS/s successive approximation register (SAR) analog-to-digital converter (ADC) is realized in 90 nm CMOS process. With the proposed logic control scheme and novel switch-driving register (SDR), the proposed SAR ADC achieves high conversion rate, low power, leading to SNDR of 59 dB and SFDR of 72.6 dB at 100 MS/s with 49.7 MHz input. The figure-of-merit (FoM) is 39.1 fJ/conversion-rate at 100 MS/s with a power consumption of 2.87 mW.

1. INTRODUCTION

With the feature size of CMOS devices scaled, design techniques for high speed SAR ADCs are being actively researched today in efforts to extend the advantages of a low-power characteristic to high speed applications. An effective design technique for high speed SAR ADC is the use of time-interleaving [1], but it suffers from matching problems between channels such as offset, gain, and sample-time skew often require complicated calibration. Another approach uses dynamic registers with asynchronous operation to reduce clock power and increase the conversion speed [2, 3].

Compared to synchronous processing, asynchronous processing technique optimizes the internal comparison time between subsequent bits. Therefore, it substantially shortens the conversion time. Nevertheless, the propagation delay in the successive approximation (SA) loop is also one of the dominant speed limiting factors, it can be reduced by optimizing the implementation of the SA logic [4].

This paper proposes a novel logic control scheme to reduce SA loop delay resulting in fast conversion operation. The remainder of the paper is organized as follows: Section 2 discusses the architecture analysis of the SAR ADC in order to obtain optimum performance. Section 3 introduces the circuits and implementation of building blocks of the proposed ADC. Layout of the proposed SAR ADC and simulation results are presented in Section 4 and conclusions are made in Section 5.

2. ADC ARCHITECTURE

The architecture of conventional SAR ADC is illustrated in Fig. 1(a) with the key blocks of capacitor network, comparator, SA control and the basic processing loop. As show in Fig. 1(a), the pulse generator generates the comparator control clock (CLKC) to trigger the comparator to regenerate and reset. After completing the comparison, a valid signal is generated to trigger the shift register to generate multi-phase clocks for switch-driving register (SDR). Then the comparison results are transmitted to switch-driving register and the outputs of the SDR are used to determine charging or discharging the DAC capacitor array before the next comparison. The key timing path is from the start of the comparison to the completely settlement of the DAC, the propagation delay in the critical path is one of the dominant speed limiting facts. In order to reduce the SA cycling time in SAR ADC, the timing path should be shortened. The proposed SAR ADC applies optimized

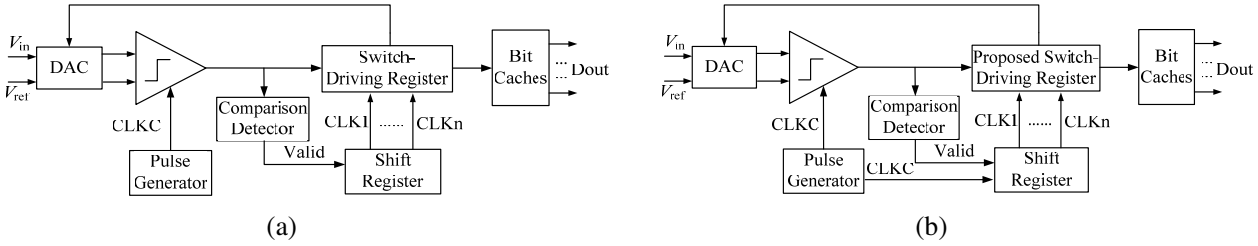

Figure 1: Block diagram of (a) conventional SAR ADC architecture; (b) SAR ADC architecture utilizing proposed logic control scheme.

logic control schemes to enhance the conversion speed, the block diagram of SAR ADC utilizing proposed circuit techniques is shown as Fig. 1(b).

3. CIRCUIT IMPLEMENTATION

3.1. Reference DAC

Figure 2 shows the detail schematic of the reference DAC. The DAC serves two purposes in a SAR converter: 1) it samples the input signal; 2) it generates a residue voltage between the input and current digital estimate. In the past few years, several power-efficient switching sequences for the capacitive DAC have been proposed such as the energy-saving, monotonic, and V_{cm}-based switching sequences [5–7].

A monotonic capacitor switching procedure is implanted during bit cycling in order to decrease the power consumption. In the first comparison, all bottom plates of these capacitances are connected to V_{refn}. The capacitors use the top plates to sample input signal and the MSB is determined by comparing the top plate's voltages directly without any change in the reference DAC. The MSB will be set to 1, if V_{DACP} is higher than V_{DACN}. Otherwise, the MSB is 0. Then the MSB triggers the SAR logic to control the reference switching of the DAC. If the MSB is 1, the capacitance C_{N1} is switched to V_{refp}. Otherwise, the capacitance C_{P1} is switched to V_{refp}.

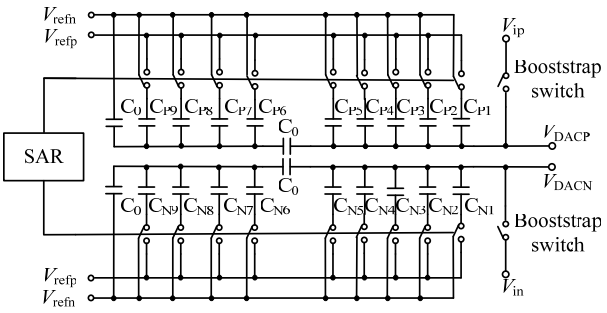

Figure 2: Schematic of the reference DAC.

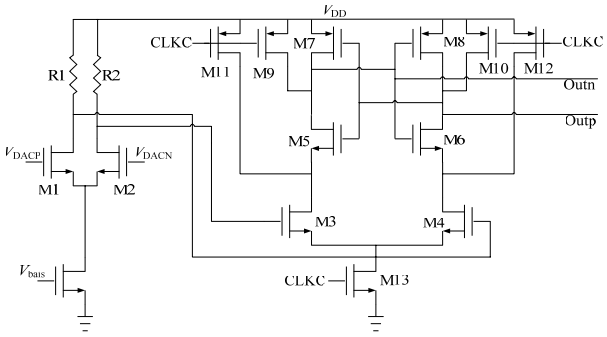

Figure 3: The schematic of the comparator.

3.2. Comparator

The schematic of the comparator is shown in Fig. 3, which consists of a pre-amplifier and a dynamic latched comparator. The pre-amplifier is used to block the kickback noise and enhance the comparison speed. During the conversion phase, the input voltage of the comparator approach V_{refp}. For optimum speed and yield of dynamic comparator, the input common-mode voltage is about 70% of the supply voltage [8]. Therefore, the comparator uses an N-type input pair rather than a P-type one. When CLKC goes low, the comparator is at the reset state and the outputs of the comparator are reset to high. When CLKC goes high, the input pair compares the two input voltages. According to the comparison result, the latch regeneration forces one output to high and the other to low. The dimensions of those MOSFETs in the comparator are carefully designed to satisfy the speed requirement.

3.3. Proposed Logic Control Scheme

In the proposed SAR ADC, the regeneration of the comparator and the operation of the shift register and the SDR are simultaneous. The timing diagram of the proposed SAR ADC is shown in Fig. 4(a). When CLKC goes high, the comparator goes in the regenerate state and conversion phase is beginning. It also triggers the shift register to generate multi-phase clocks for SDR. Then the SDR is enabled. Thus, the comparison results are direct transmitted to determine charging or discharging the DAC capacitor array before the next comparison without waiting for the completion of the comparison. The valid signal is only used to disable the corresponding-phase clock and is not in the key timing path. So the key path of the SA loop is shortened in the proposed SAR ADC. In addition, a novel SDR is proposed to further improve the conversion speed as shown in Fig. 4(b). RST is the reset signal. During the sample phase of the DAC, the output of the SDR is reset to low. The input of SDR is the output of the comparator. The outputs of SDR are connected to a serial of inverters used to drive the corresponding capacitors in the reference DAC. As a result, the

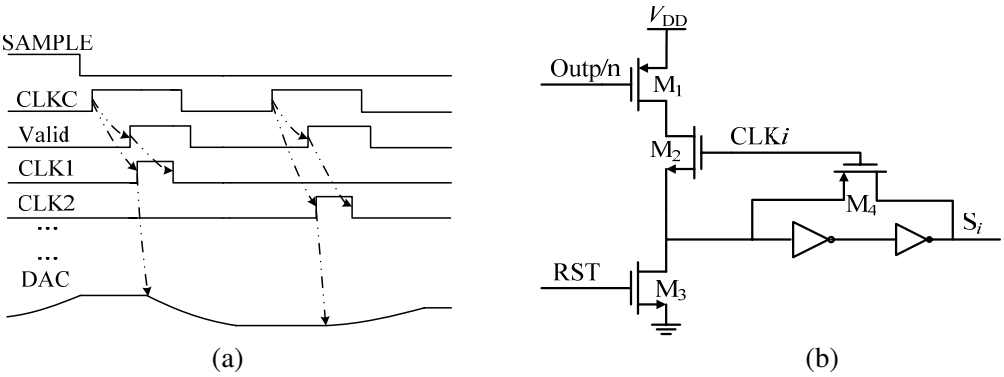

Figure 4: (a) The timing diagram of the proposed SAR ADC; (b) the proposed switch-driving register.

dynamic latch transfers comparator's output to DAC directly when the comparator starts to latch. This eliminates the time delay from the comparator to generating a valid signal.

4. LAYOUT AND SIMULATION RESULTS

The prototype ADC is realized in 90 nm CMOS process. Fig. 5(a) shows the layout of the proposed SAR ADC. At 100 MS/s operation under a 1.2 V supply, the total power consumption is 2.87 mW. Unit capacitance of the DAC is 20 fF, and the total input capacitance is about 640 fF. Fig. 5(b)

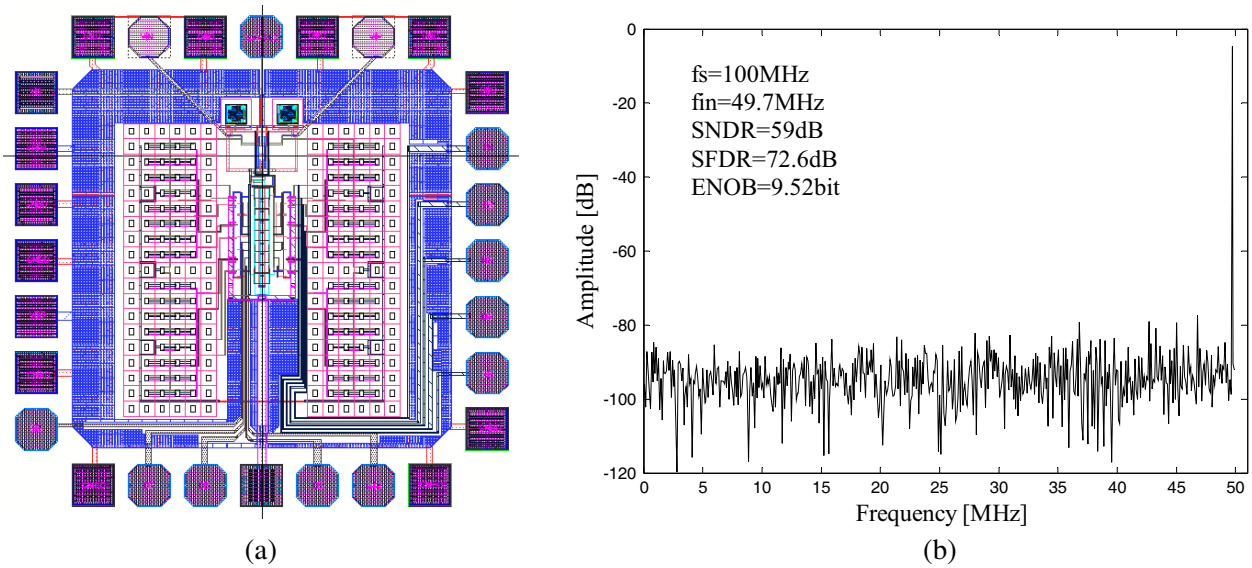

Figure 5: (a) Layout of the proposed ADC; (b) simulation results at 49.7 MHz (0.9 full-scale sine) input and 100 MS/s.

Table 1: Summary of this design and comparison with the others.

Ref	[3] TVLS	[6] JSSCC	[7] JSSCC	This work
Architecture	SAR	SAR	SAR	SAR
Technology	90 nm	0.13 µm	90 nm	90 nm
Resolution (bit)	10	10	10	10
Sample Rate (MS/s)	30	50	100	100
Supply Voltage (v)	1	1.2	1.2	1.2
Power (mw)	0.98	0.826	3	2.87
SNDR (dB)	56.89	57	56.6	59
SFDR (dB)	68.65	65.9	71	72.6
ENOB (bit)	9.16	9.18	9.1	9.52
FoM (fJ/step)	57	29	55	39.1

shows the ADC dynamic performance. The SNDR and SFDR at 49.7 MHz input are 59 dB and 72.6 dB. To evaluate the overall performance of the ADC, we use a FoM equation defined as

$$\text{FoM} = \text{Power}/(2\text{ENOB} * fs) \tag{1}$$

where fs is the sampling frequency and ENOB is the effective number of bits. The resultant FoM is 39.1 fJ/conversion-step.

5. CONCLUSION

This paper presents a 10-bit 100 MS/s SAR ADC. The propagation delay of the SA loop is reduced by the proposed logic control method, which enhances the conversion speed of the SAR ADC. A new switch-driving register is proposed to further improve the conversion speed. The performance summary and comparison with state-of-the-art ADCs are shown in Table 1.

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