A 45-GHz CMOS Low-power LNA Using Active Feedback

Li Ma, **Zhigong Wang**, **Jian Xu**, **and Xixi Chen**
Institution of RF-&OE-ICs, Southeast University, Sipailou 2, Nanjing 210096, China

Abstract— A 45 GHz low power millimeter-wave (MMW) low noise amplifier (LNA) using 40 nm CMOS process is presented in this paper. The LNA comprises three stages. The first stage adopts the active feedback structure for good input matching. The output matching employs an L-type matching network. Simulation results show that both S_{11} and S_{22} are less than -18 dB at 45 GHz. A cascode structure is adopted in the third stage for better reverse isolation. The LNA consumes 18.7 mW under a 1.1-V voltage supply, achieving a maximum S_{21} of 17.9 dB. The minimum NF is 5.7 dB at 42.5 GHz. The simulation results show that the proposed LNA is promising for the 45-GHz application.

1. INTRODUCTION

In recent years, MMW circuits have been studied widely for its capability of high data rate communication. For example, the frequency band of $76 \sim 81$ GHz is for automotive radar and 60 GHz is a promising band for high speed wireless communication [1, 2]. Q-LINKPAN which has been included in IEEE 802.11aj (45 GHz) Task Group is a newly proposed communication standard working within the 40–50 GHz [3].

An LNA that provides a good noise performance, excellent matching and enough gain is necessary in an MMW receiver. The development of deep submicrometer CMOS process makes it possible to implement a CMOS MMW LNA. Some MMW LNAs have been reported recently [4–6]. However, their power consumptions are relatively high and the matching is not satisfactory. In [6], for example, a 3-stage 79-GHz LNA is presented. Though a low NF 4.9 dB and a variable gain are achieved, the power consumption of 30.6 mW and $S_{22} < -10$ dB was not good enough. In this paper, a-45 GHz low power 3-stage LNA with excellent matching is designed in 40 nm CMOS process. An active feedback is adopted for the input matching.

2. CIRCUIT DESIGN

Considering the high transition frequency of the 40 nm CMOS process, excellent input matching is possible to achieve by feedback. The resistive feedback LNA in Fig. 1(a) and active feedback LNA in Fig. 1(b) are widely used in wideband LNA [7]. Ignoring the parasitic capacitors, the input impedance of the resistive feedback LNA is,

$$R_{in} \approx \frac{1}{g_{m1}} \tag{1}$$

where g_{m1} is the transconductance of M_1.

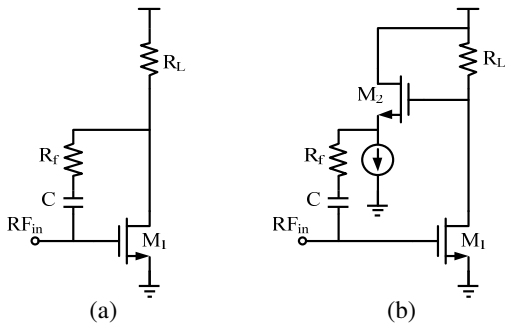

Figure 1: (a) Resistive feedback LNA; (b) Active feedback LNA.

Assuming that M_2 performs as an ideal buffer, the input impedance of the active feedback LNA is,

$$R_{in} = \frac{R_f}{1 + g_{m1} R_L} \tag{2}$$

Equation (1) shows that the transconductance is restricted to 20 mS to meet the input matching requirement. The first stage's noise performance which dominates the whole circuit's noise figure (NF) is mainly decided by g_{m1}. Therefore, the NF cannot be lowered by increasing the aspect ratio of M_1 or the current consumption. The output impedance of the active feedback LNA is R_L, while the output impedance of resistive feedback LNA is,

$$R_{out} \approx R_f // R_L \tag{3}$$

Equation (3) shows that the output impedance is affected by the feedback resistor. It makes the matching between the output of the first stage and the input of the second stage more complex. Therefore, the active feedback in Fig. 1(b) is preferred.

Figure 2 shows the proposed 3-stage LNA employing active feedback structure in the first stage. Different from the second and third stage, the bias voltage of M_1 is through an inductor L_1. This bias inductor not only provides high impedance at the frequency concerned but also constructs a parallel resonant network with the parasitic capacitor C_{gs1} of M_1. This network filter out the signal out of band. The small signal circuit of the first stage is depicted in Fig. 3. The input impedance is derived as,

$$Z_{in} = j\omega L_1 // \frac{1}{j\omega C_{gs1}} // \frac{R_f}{1 + g_{m1} \cdot (j\omega L_2 // j\omega C_L)} \tag{4}$$

To ensure the input impedance matching, the resonant frequency of the two LC network are both configured at about 45 GHz. A cascode structure is adopted in the last stage for better isolation between the output and the input. The aspect ratio of M_5 is half of M_4 to minimize the parasitic capacitor which determine the reverse isolation. L_4 and C_5 comprise an L-type output matching network.

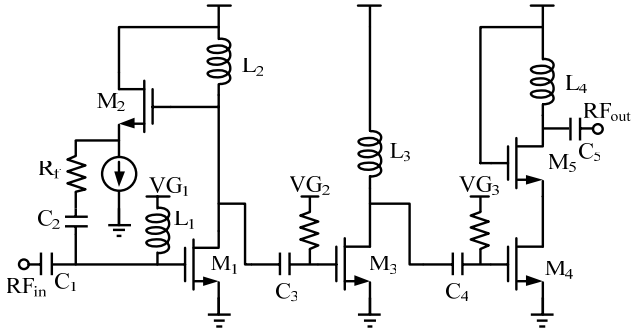

Figure 2: Proposed 3-stage LNA.

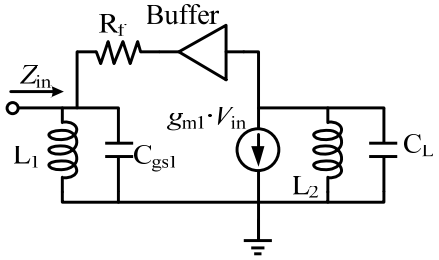

Figure 3: Small signal circuit of input network.

3. SIMULATION RESULTS

The proposed LNA is designed in a 40 nm CMOS process. The die area of the layout shown in Fig. 4 is 0.78 mm × 0.7 mm. The minimization of parasitic resistance and capacitance are critical to ensure that the LNA will work well in an MMW frequency range. Therefore, the layout has been designed meticulously. Simulations have been carried out using Cadence Spectre. The total current is 17 mA under a 1.1 V voltage supply.

Figure 5 shows the LNA's S-parameter and NF. The simulation results in Fig. 5(a) shows that $S_{11} < -10\,\text{dB}$ through the whole band of 40–50 GHz. and it achieves an S_{11} of $-18.8\,\text{dB}$ and an S_{22} of $-25\,\text{dB}$ at 45 GHz. The frequency band of $S_{22} < -10\,\text{dB}$ is $42 \sim 48.5\,\text{GHz}$. The maximum S_{21} is 17.9 dB at 42 GHz. The NF is less than 7 dB in the frequency band concerned. Table. 1 shows the simulation results summary and comparison with published works.

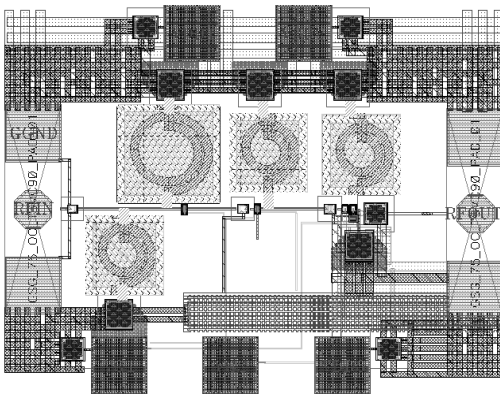

Figure 4: Layout of LNA.

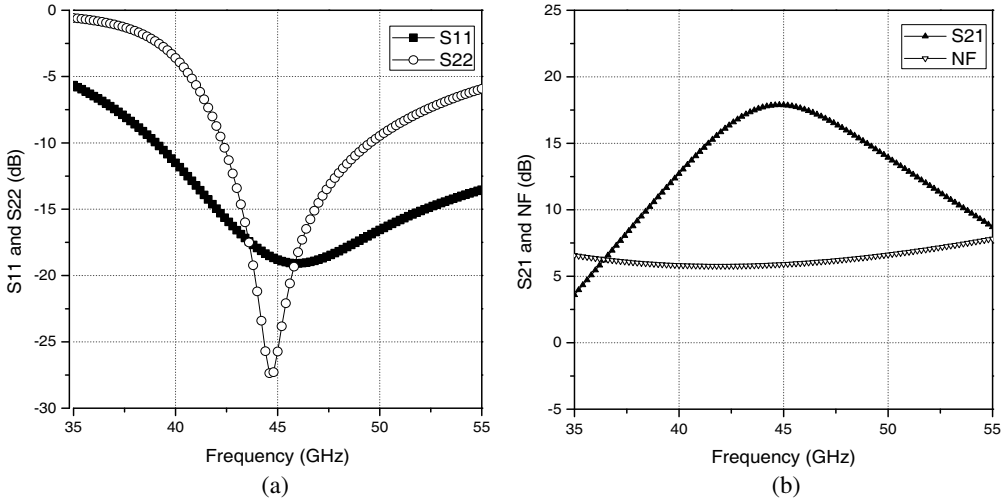

Figure 5: (a) Simulated S_{11} and S_{22}; (b) Simulated S_{21} and NF.

Table 1: Simulation results summary and comparison.

	This Work	[1]	[5]	[6]
Process (nm)/VDD (V)	40/1.1	90/NA	65/1.5	28/0.9
3 dB BW (GHz)	$41.5 \sim 49$	$77 \sim 81$	$2.1 \sim 39$	$74 \sim 84$
NF_{min} (dB)	5.7	6.2	4.5	4.9
$S_{21\text{max}}$ (dB)	17.9	13.5	11.5	23.8
IIP_3 (dB)	-9	-11	NA	NA
Power (mW)	18.7	21.1	25.5	30.6

4. CONCLUSIONS

In this work, we demonstrate a low-power MMW LNA in a 40-nm CMOS process. The first stage of the LNA adopts the active feedback structure for a better input matching. A cascode structure is employed in the last stage for better reverse isolation. The LNA consumes 18.7 mW under a

1.1 V voltage supply. Compared to the published MMW LNAs, this work achieves the minimum power. The maximum S_{21} is 17.9 dB at 45 GHz. The LNA achieves a minimum NF of 5.7 dB at 42.5 GHz. The simulation results shows that the proposed LNA is promising for the Q-LINKPAN application.

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