A 2 GSps 8 bit Folding & Interpolation ADC in 90 nm CMOS Technology

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Abstract— A single channel 2 GSps, 8 bit folding and interpolation (F&I) analog-to-digital converter (ADC) designed in TSMC 90 nm CMOS technology was presented in this paper. The ADC utilized cascaded folding architecture, which incorporated an additional inter-stage sample-and-hold amplifier between the two stages of folding circuits to enhance the quantization time. A pipelined track-and-hold amplifier (THA) with bootstrapped switch was taken as the front-end THA to improve its performance. The foreground digital assisted calibration was also employed in this design to correct the error of zero-crossing point caused by the circuit offset, thus to improve the linearity of the ADC. Chip area of the whole ADC including pads is 930 µm × 930 µm. Post simulation results demonstrate that under a single supply of 1.2 Volts, the ADC consumes 210 mW. For the clock of 2 GHz, the signal to noise and distortion ratio (SNDR) is 45.93 dB for Nyquist input signal frequency.

1. INTRODUCTION

Ultra-high-speed (GSps), medium resolution Analog-to-digital converters (ADCs) are the key element in many electronic systems, such as communication system, test equipmentradar and radio astronomy system. With the development of technology, in many of these systems, signal has a bandwidth of over 1 GHz, such as the ultra-wide-band (UWB) technology. So, research of ADCs which has a sampling rate over 2 GSps is of great significance. Flash and Folding ADC are the primary candidates for GSps applications due to their high conversion speed and low latency. Although the flash architecture has been used in the highest speed ADCs, it has the severe disadvantage that it requires 2^N comparators for N bits of resolution, which results in a substantial area and power penalty starting at the 8 bit level. As a result, pipelined Folding and Interpolation (F&I) was adopted in this design of 2 GSps, 8 bit ADC.

In this design, cascaded folding architecture was taken to enhance the quantization time. Folding and interpolation factors were selected to be 3×3 and 2×8 to balance system area and performance. Foreground digital assisted calibration was adopted to eliminate device mismatch, the impact of gain error and the mismatch error of the channel.

In Part 2, key circuits and digital calibration will be presented. Part 3 gives layout and system simulation results. Part 4 is the conclusion and Part 5 is the acknowledgement.

2. CIRCUIT OF THE PROPOSED ADC

From Fig. 1 it can be seen that the proposed ADC is a single channel circuit. The upper part is the main circuit and the under part is the calibration circuit. For the main circuit, the coarse and the fine channel quantify the signal from the front-end track-and-hold amplifier (THA) respectively and deliver the quantization signal to the 8 D Flip-Flop (DFFs) to get the final results. The Fine channel is much more complicated than the coarse channel. It is composed of 19 preamps (1 for redundancy), two F&I stages (6 for the first stage with folding factor = 3 and interpolation factor = 2; 4 for the second stage with folding factor = 3 and interpolation factor = 8) and 12 inter-stage sample and hold amplifier (SHA) to enhance the quantization time, 32 comparators, 32 spark code elimination circuit and fine coding circuit. The coarse channel is composed of 6 preamps, 6 comparators, 1 synchronization circuit to make sure the result is right and coarse coding circuit.

The under part is the calibration circuit and it includes logic control, counter, DFF array and digital-to-analog converter (DACs). It will be explained more in Chapter 2.3.

2.1. The Front-end THA

For gigahertz sampling rate operation, it is far better to have a front-end THA as it can improve the dynamic performance of an ADC [1]. By holding the analog sample static during digitization,

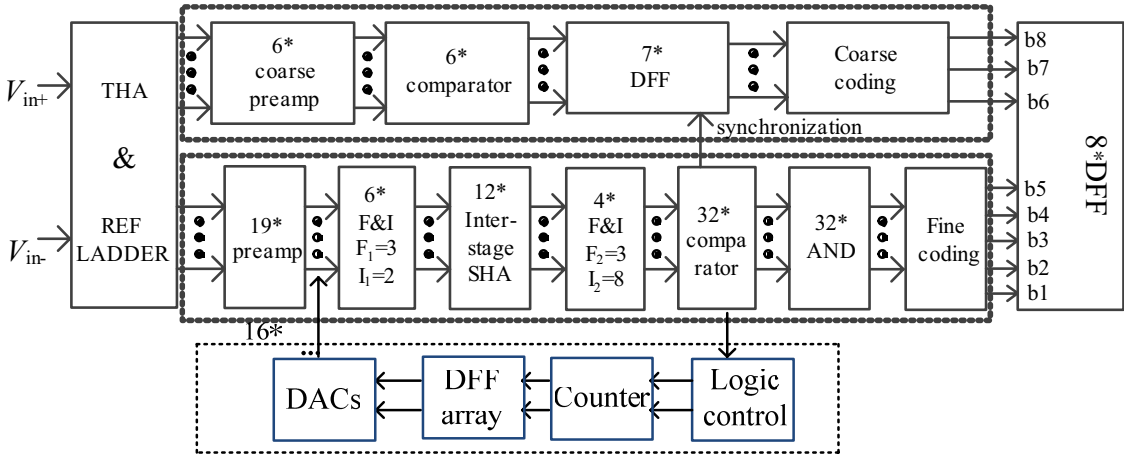

Figure 1: Diagram of the proposed ADC.

the THA largely removes errors due to skews in clock delivery to a large number of comparators, signal-dependent nonlinearity, and aperture jitter.

The THA designed takes the open-looped architecture, presented in Fig. 2. The bootstrapped switch is adopted as its equalized resistance has less to do with the input voltage, thus to improve THA's linearity. Also, its over-drive voltage is larger than the normal MOS switch, so the equalized resistance is smaller, and the sampling rate is improved.

As the designed THA should be working at 2 GSps while having a resolution of over 8 bit, a second stage THA was designed after the regular THA, thus making a novel pipelined THA, shown in Fig. 2. The second stage THA tracks and holds the signal of the first stage THA. As the second stage THA's input signal is less varying as the original input signal, the linearity requirement of the second stage is much easier to realize than the first stage. To gain a large bandwidth for the THA, the second stage also takes the bootstrapped switch, but much easier than the first one.

The simulation results demonstrate that the pipelined THA has a good performance. For clock of 2 GHz, input signal of 1 GHz, its 128 point Fast Fourier Transform (FFT) spectrum was shown in Fig. 3. It can be seen that the THA's Signal to Noise and Distortion Ratio (SNDR) is 61.5 dB, suited for the ADC.

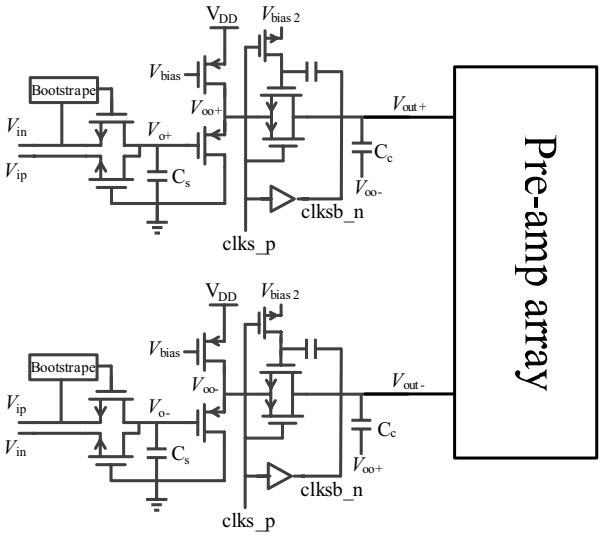

Figure 2: The designed pipelined THA.

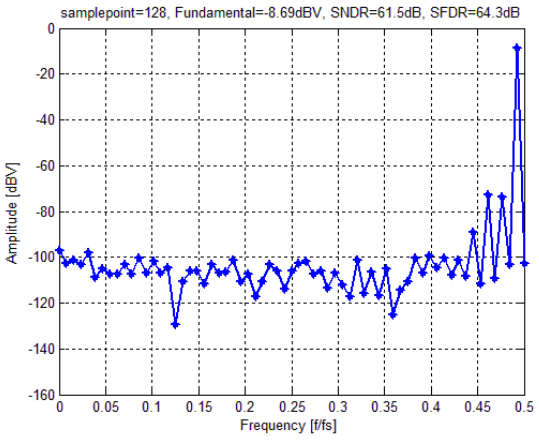

Figure 3: Output spectrum (Nyquist input@2 GSps).

2.2. Folding and Interpolation Network

With the analog pre-processing, the F&I architecture can better balance ADC's area, power and performance. The pre-amplifier array generates the original zero-crossing points, but never enough or it will be the flash architecture. As can be seen in Fig. 1, the two-stage cascaded F&I was taken in this design with inter-stage SHA circuit in between. These two stages are similar so it can be discussed together. With the help of F&I network, enough zero-crossing point will be generated while the system area and power is much smaller than its flash counterpart.

The first key element in designing the folding circuit is that it should have enough bandwidth to make sure signal can be settled within the limited time especially for ultra-high-speed ADCs. Second, it should have a certain gain to suppress the offset of next stage. Third, its offset should be controlled within a limited amount.

Figure 4 is the proposed F&I network. M1–M6 is the input differential pair as the folding factor is 3. M7 and M8 have two roles, first to insulate the signal from the input. Second, as the drain of three MOSFET is connected, its output capacitance is very large. With small sized M7 and M8, the bandwidth of the folding circuit can be increased. The AC simulation of the folding circuit is shown in Fig. 5. The gain is 5.38 dB and its −3 dB bandwidth is 4.9 GHz, suited for the ADC.

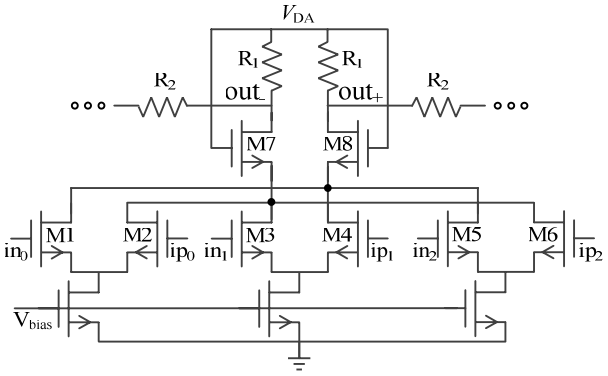

Figure 4: The designed F&I circuit.

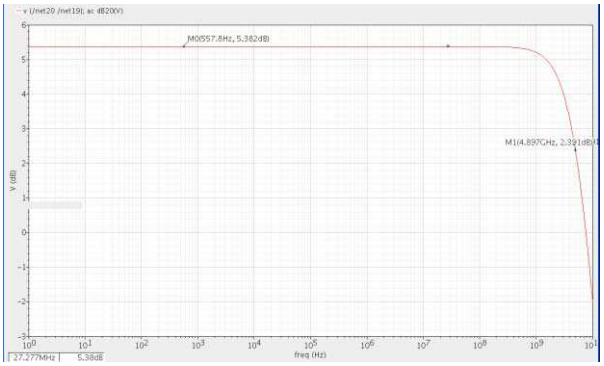

Figure 5: AC simulation result of folding circuit.

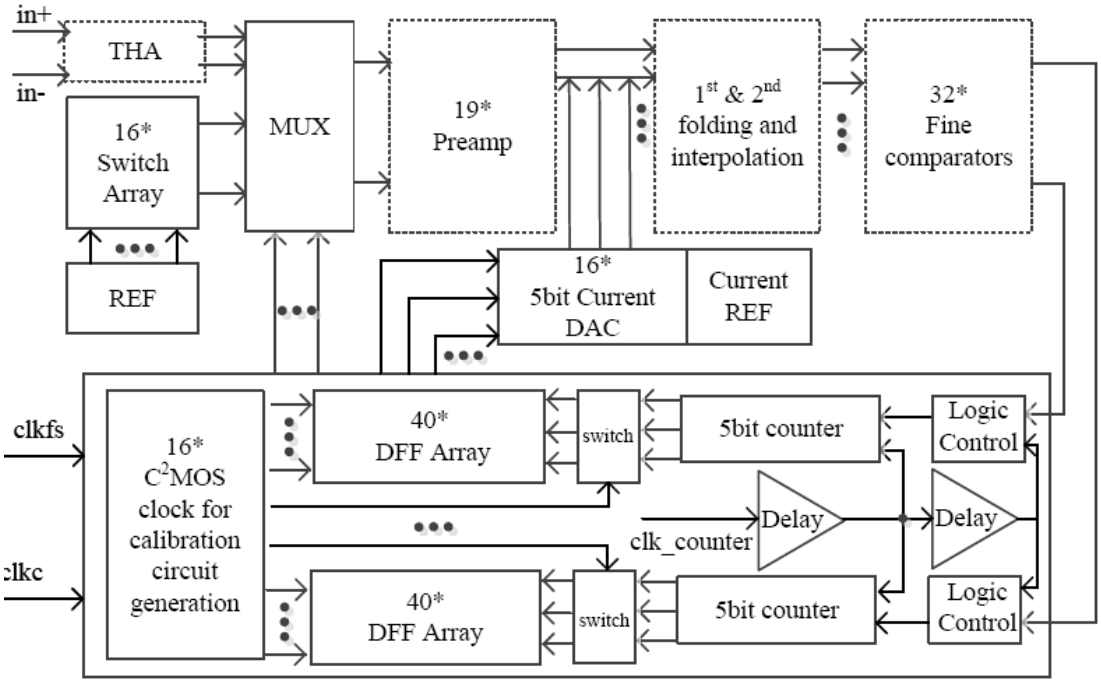

Figure 6: Diagram of digital assisted calibration.

2.3. Foreground Digital Assisted Calibration

As the main error in folding and interpolation architecture is the offset, and it will hardly change according to the temperature and external circumstance. Once the ADC is made, the offset is fixed. So, the foreground digital assisted calibration was adopted in this design. The actual offset can be measured and stored in the DFF array. When the ADC is working, the offset stored will be used to compensate for the real offset of the circuit, thus the offset is eliminated and the linearity is improved.

Figure 6 presents the diagram of the digital assisted calibration. From this figure, it can be seen that the offset of all the analog processing blocks, including pre-amplifier, inter-stage SHA, two stages of folding and interpolation circuit can be measured and stored. The calibration circuit contains three key sub-circuits as (1) the clock generation circuit for calibration. Here, the C^2MOS circuit is adopted as it can generate 16 ways of calibration clock without overlapping. (2) The DFF array can be used to store the measured offset in the calibration phase. (3) The current DAC convert the stored digital offset to analog current and directly inject it to the output of pre-amplifier. In this way, it achieves the subtraction between the offset voltage and the stored offset voltage, thus the compensation is done and the linearity is improved.

3. LAYOUT AND SIMULATION RESULTS

To avoid the interference between analog and digital parts and obtain better performance, the power and ground patterns in analog and digital modules are separated. Fig. 7 is the layout of the ADC. Chip area is 930 µm × 930 µm with pads.

Figure 8 shows the post simulation result of 128-point FFT output spectrum. From the figure,

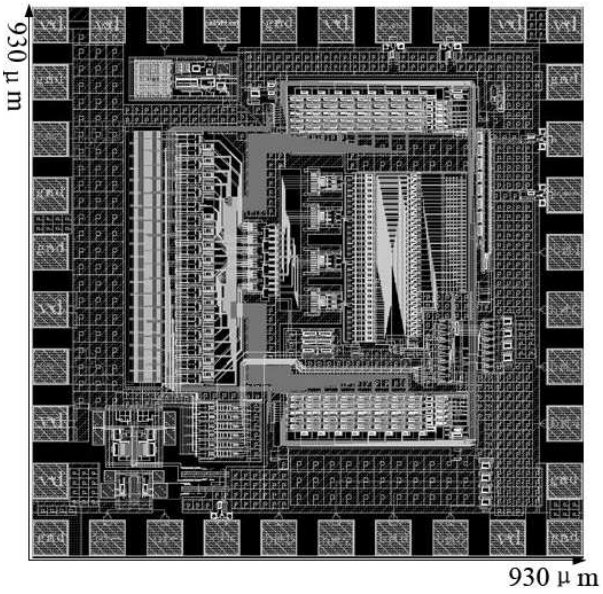

Figure 7: Layout of the ADC.

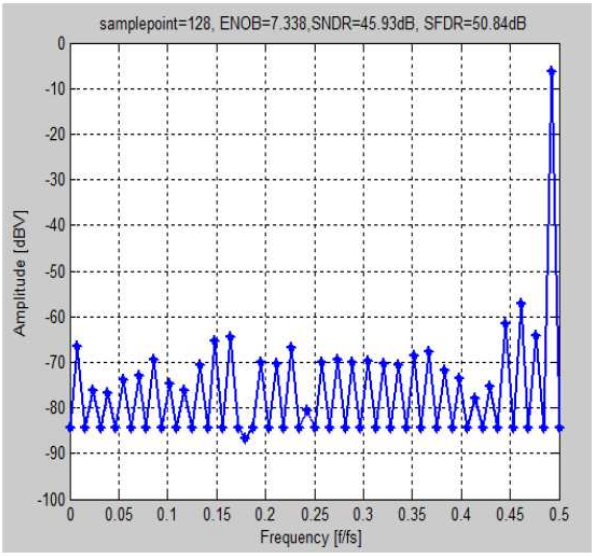

Figure 8: Output spectrum (Nyquist input @2 GSps).

Table 1: Post simulation results of F&I ADC and comparison with others.

Performance	[2]	[3]	[4]	[5]	This work
Technology	0.18 µm CMOS	0.18 µm CMOS	90 nm CMOS	90 nm CMOS	90 nm CMOS
Supply (V)	1.8	1.8	1	1.2	1.2
Clock (GHz)	1.6	1	2.7	1	2
SFDR (dB)	56	68.6		28.87	50.84
SNDR (dB)	46	56.5	33.6	27.35	45.93
Power (mW)	774	1260/channel	50	7.65	210
Area (mm^2)	3.6	49 (dual ADC)	0.36	0.063	0.865

it can be seen for Nyquist input signal ($f_{\text{in}} = 1\,\text{GHz}$) @2 GSps, the Spurious Free Dynamic range (SFDR) is 50.84 dB and the SNDR is 45.93 dB, so the Effective Number Of Bit (ENOB) is calculated to be 7.338 bit. The result demonstrates that the ADC has a good dynamic performance.

The performance of the designed F&I ADC and the comparison with other published ones (SNDR and SFDR for Nyquist sampling in [2–4], 260 MHz@1 GSps in [5]) are listed in Table 1.

4. CONCLUSION

In this paper, a 2 GSps, 8 bit cascaded folding and interpolation ADC with foreground digital assisted calibration in TSMC 90 nm CMOS technology is presented. The ADC consumes an area of 930 µm × 930 µm with pads and achieves a 7.338 bit of ENOB at Nyquist input frequency with a power consumption of 210 mW from a single supply voltage of 1.2 Volts. The simulation results demonstrate that the designed ADC is suitable for ultra-high-speed, medium resolution signal processing systems.

ACKNOWLEDGMENT

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REFERENCES

1. Razzaghi, A., "A single-channel 10 b 1 GS/s ADC with 2-cycle latency using pipelined cascaded folding architecture," PhD Thesis, UCLA, 2008.
2. Taft, R. C., C. A. Menkus, M. R. Tursi, et al., "A 1.8-V 1.6 GSample/s 8-b self-calibrating folding ADC with 7.26 ENOB at Nyquist frequency," *IEEE Journal of Solid-State Circuits*, Vol. 39, No. 12, 2107–2115, 2004.
3. Taft, R. C., P. A. Francese, M. R. Tursi, et al., "A 1.8 V 1.0 GS/s 10 b self-calibrating unified-folding-interpolation ADC with 9.1 ENOB at Nyquist frequency," *IEEE Journal of Solid-State Circuits*, Vol. 44, No. 12, 3294–3304, 2009.
4. Nakajima, Y., A. Saaguchi, T. Ohkido, et al., "A background self-calibrated 6 b 2.7 GS/s ADC with cascade-calibrated folding-interpolating architecture," *IEEE Journal of Solid-State Circuits*, Vol. 45, No. 4, 707–718, 2010.
5. D'Amico, S., G. Cocciolo, A. Spagnolo, et al., "A 7.65-mW 5-bit 90-nm 1 Gs/s folded interpolated ADC without calibration," *IEEE Transactions on Instrumentation and Measurement*, Vol. 63, No. 2, 295–303, 2014.