A Spread Spectrum Clock Generator Using Discontinuous Modulation Technique for Reduction of Time Interval Errors

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Abstract— In this paper, we propose a novel discontinuous spread spectrum clock generator with a low maximum time interval error (MTIE) and low electromagnetic interference (EMI). The proposed circuitry was fabricated with 0.35 µm CMOS process and operated with 3.3 V supply voltage at the average center frequency of 100 MHz. The measured results showed the MTIE of 11.59 ns with the EMI reduction of 14.57 dBm.

1. INTRODUCTION

Nowadays, faster operating speed of automotive electronic units brings about such serious problems as functional failures due to electromagnetic interference at high frequency [1, 2]. An effective solution to diminish EMI is to modulate system clock frequency, which is known as a spread spectrum clock (SSC). This method reduces EMI by spreading energy of discrete frequency harmonics over a wide range of frequencies. However, asynchronous serial data protocols in vehicle networks require a strict time interval error (TIE) range because receivers in asynchronous CAN circuitry may detect wrong data when the TIE is out of range [2].

Several methods have been reported to find efficient solutions considering trade-offs between the TIE and EMI reduction. One method solving the TIE issue is to reduce a modulation index. While this approach reduces the MTIE, it degrades the EMI reduction [3]. Another method reported in [2, 4] can reduce the MTIE without sacrifice of EMI performance. However, its implementation needs complex and large additional circuitry. In this paper, we propose novel SSC technique which satisfies requirement on the MTIE and reduces EMI effectively in asynchronous vehicle networks.

2. DESIGN DESCRIPTIONS

2.1. EMI Reduction and MTIE

When a conventional triangular modulation profile is adopted for SSC, the reduction of EMI peaks can be estimated by Equation (1) [5]. In Equation (1), f_c, A_{mo} and F_{mo} are center spread frequency, modulation depth, and modulation frequency, respectively. In the center-spread method, the TIE is varied from 0 to MTIE within one modulation cycle. The MTIE level is also given in Equation (1) as a function of A_{mo} and F_{mo} [2, 5].

$$\text{EMI Peak Reduction} = 10 \times \log\left[\frac{A_{mo} \times f_c}{F_{mo}}\right], \quad \text{MTIE} = \frac{A_{mo}}{8 \times F_{mo}} \tag{1}$$

$$\text{EMI Peak Reduction} = 10 \times \log\left[8 \times \text{MTIE} \times f_c\right] \tag{2}$$

Equation (2) shows EMI peak reduction expressed with MTIE and f_c. In general, the higher MTIE gives rise to the higher EMI peak reduction as shown in Equation (2). However, requirement on the MTIE limits the use of SSC for asynchronous interfaces. Therefore, a new method to effectively reduce MTIE becomes indispensable in automotive networks requiring low EMI generation.

2.2. Proposed Discontinuous Modulation Technique

Figure 1 shows concepts of the conventional SSC and the proposed discontinuous spread spectrum clock (DSSC). Figure 1 also shows comparison between theoretical TIE plots. The proposed method is based on up-spread spectrums while the conventional SSC uses the center-spread spectrums with respect to the center frequency (Non-SSC frequency). In the conventional method, the modulation index (A_{mo}/F_{mo}) should be properly reduced to comply with the allowed MTIE. On the other hand, the proposed method can control TIE within the allowed MTIE by resetting TIE with selection of its half-frequency clock whenever the TIE runs over one clock cycle. Therefore, the proposed modulation depth A_{mo_p} can be larger than A_{mo_c} of the conventional SSC. The proposed DSSC technique with high modulation depth can reduce EMI effectively while maintaining the targeted MTIE.

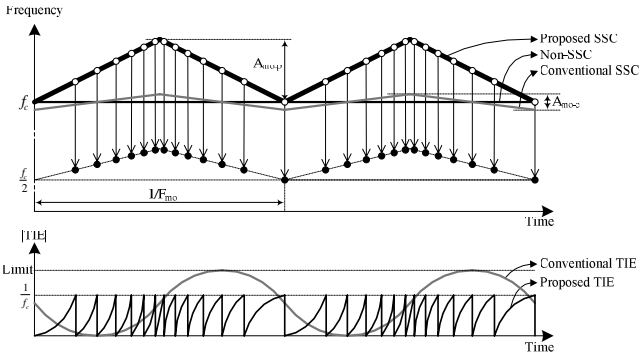

Figure 1: Comparison between the conventional SSC and the proposed DSSC.

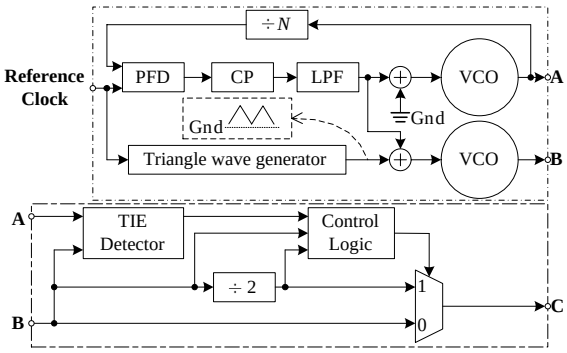

Figure 2: Block diagram of the proposed discontinuous modulation SSC (signal A: Non-SSC, signal B: Up-SSC, signal C: DSSC).

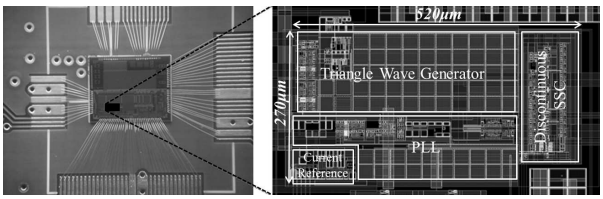

Figure 3: Test chip photograph and layout.

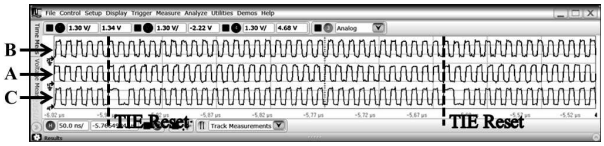

Figure 4: Measured discontinuous modulation SSC (signal A: Non-SSC, signal B: Up-SSC, signal C: DSSC).

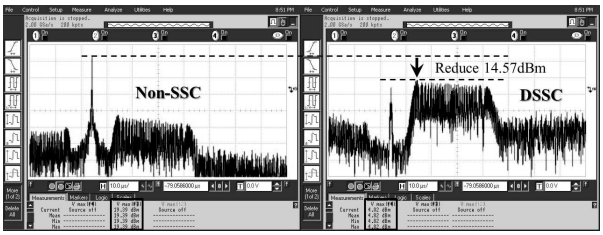

Figure 5: Measured spectrums of the output signals (DSSC and Non-SSC).

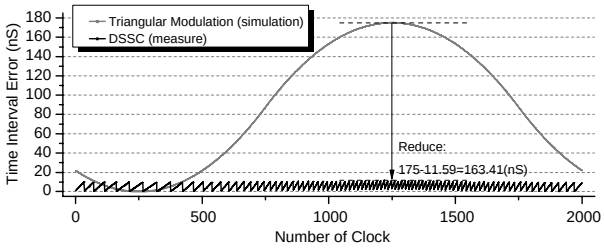

Figure 6: Measured time interval error.

2.3. Circuit Descriptions

Figure 2 shows the block diagram of the proposed discontinuous modulation SSC which consists of a PLL (Non-SSC) block, an up-spread spectrum clock (Up-SSC) block, a TIE detector, and a tiny control logic block. The Non-SSC clock is generated at the node A and the Up-SSC is simultaneously generated at the node B. In the next stage, the TIE detector compares the signal B with the signal A. It checks out whether the accumulated TIE is within one clock cycle. The detected signal is transferred into the Control Logic. The Control Logic and MUX select Up-SSC clock or its half-frequency clock generated through the 1/2 divider. If the accumulative TIE reaches one clock cycle, the TIE is reset to zero by selection of the half-frequency clock. The repeating reset sequence can always keep the MTIE within one clock cycle. The photograph of the test module and the chip layout are shown in Figure 3. The designed chip size is 520 μm × 270 μm. The chip was fabricated with 0.35 μm CMOS process and operated with 3.3 V supply voltage.

3. MEASUREMENT RESULTS

The fabricated chip was tested with the modulation frequency (F_{mo}) of 50 kHz and the modulation depth (A_{mo}) of 7% with respect to the center frequency (Non-SSC frequency) of 100 MHz. Figure 4 shows the measured clocks of Up-SSC (B), Non-SSC (A), and DSSC (C). It shows that the measured DSSC (C) resets the TIE to be zero whenever the TIE of Up-SSC is accumulated over one period of Non-SSC clock. Figure 5 shows the measured EMIs of the Non-SSC and the DSSC. The EMI characteristic of the DSSC was reduced by 14.57 dBm. Figure 6 shows comparison between the

simulated TIE of the conventional SSC and the measured TIE of the DSSC under the same EMI performance. The MTIE of the proposed DSSC is improved from 175 ns to 11.59 ns; i.e., by MTIE reduction of 163.4 ns.

4. CONCLUSION

The proposed SSC with discontinuous modulation technique can reduce EMI peaks while maintaining very low TIEs compared with the conventional SSC. Therefore, this scheme is very useful to apply to asynchronous interfaces where a strict MTIE and relatively low EMI are required. The measured results show that the EMI level is reduced by 14.57 dBm compared with the Non-SSC and the MTIE is 11.6 ns at the target frequency of 100 MHz.

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