High Precision Range Measurement Processor Design with Low Complexity for FMCW Radar Systems

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Abstract— The paper presents a signal processing hardware architecture with low complexity for high precision range measurement using FMCW (Frequency Modulated Continuous Wave) radar. The proposed architecture is designed based on coarse FFT processing with reduced point and a fine spectrum estimator for the specific frequency of interest. The implementation results on FPGA show that the proposed method leads to lower latency and requires fewer hardware resources than full-point FFT processing.

1. INTRODUCTION

FMCW (Frequency Modulation Continuous Wave) radar systems have been widely used for the measurement of range in a variety of industrial applications: automotive safety, traffic monitors, level gauges, security, defense seekers. Especially, level measurement is popular in almost every modern industrial plant for the measurement of bulk materials [1]. That is, digital level measurement based on FMCW radar is a trend because the digital approach is more flexible and program updates are very easy [2, 3].

In FMCW radar, when a continuous frequency modulated microwave signal is transmitted, the receive echo signal is down-converted into the baseband by the transmit frequency [4, 5]. The difference in frequency between the transmit and the receive signals is called the beat-frequency. The beat-frequency is typically obtained using FFT (Fast Fourier Transform) processing; range measurement is calculated using the detected beat-frequency. Thus, for exact level measurement in FMCW radar, it is very important to obtain a high precision beat-frequency. That can be realized using enough sample data and many FFT points. However, in a high precision FFT processor, many hardware resources and long processing time are required due to the increased computational complexity.

In this paper, we propose a low complexity frequency measurement processor. First, using the low precision FFT processor, the coarse ROI (Range Of Interest) is detected. Then, in the ROI, the fine frequency spectrum is analyzed using a frequency spectrum estimator consisting of a complex multiplier-accumulator. Compared with traditional FFT processors, even though the performance of the proposed processor is the same, the utilized hardware resources and the processing time can be decreased.

2. PROPOSED ARCHITECTURE

The structure of the proposed processor is shown in Fig. 1. Here, $a(n)$ is the digitalized sample of the received beat-signal and n ($= 0 \sim N-1$) is the sample index of the discrete time, where N is the number of the sample.

If $a(n)$ is fully transformed by N-point FFT processing, the corresponding frequency spectrum is calculated as in Eq. (1), where d ($= 0 \sim N-1$) is the beat-frequency index and $\Delta\omega_N$ is the radian frequency step size. Thus, the detected beat-frequency is expressed as $\Delta\omega_N \cdot n_r$, where n_r is the detected frequency index. In traditional FFT processing, the time complexity is expressed as $N \cdot \log N$.

$$X(d) = \sum_{n=0}^{N-1} \left[a(n) \cdot e^{-j(\Delta\omega_N \cdot d) \cdot n} \right] = \sum_{n=0}^{N-1} \left[a(n) \cdot e^{-j\frac{2\pi \cdot d}{N} \cdot n} \right] \quad (1)$$

On the other hand, the proposed processing is divided into two steps: the coarse frequency detection part using the reduced-point FFT and the fine frequency detection part based on the FSE (Frequency Spectrum Estimation).

In the first step, the low precision FFT processing is carried out and the result $Y(m)$ is expressed as in Eq. (2). Here, m ($= 0 \sim M-1$) is the beat-frequency index, $\Delta\omega_M$ is the radian frequency step

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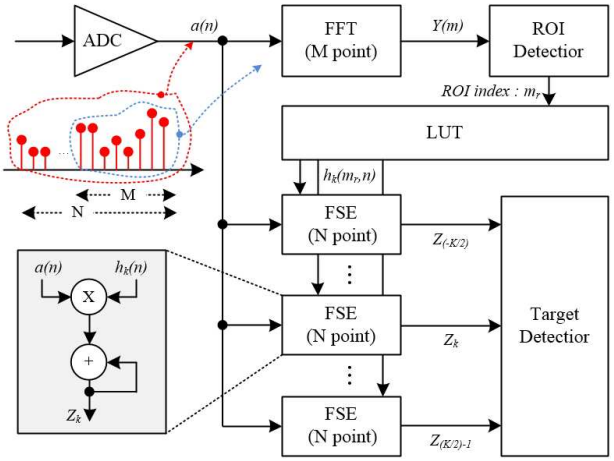

Figure 1: Structure of the proposed processor.

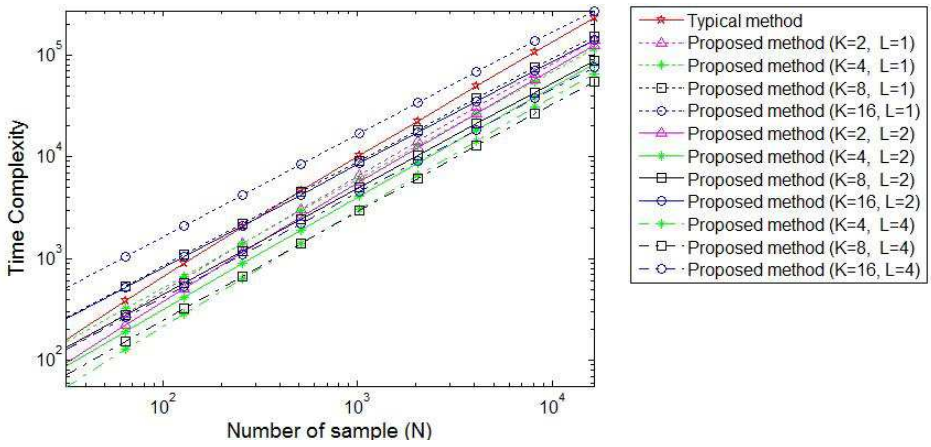

Figure 2: Time complexity comparison.

size, and M is the reduced FFT point. In this case, we define integer $K(= N/M)$, which is called 'Reduced ratio of FFT point'.

$$Y(m) = \sum_{n=0}^{M-1} \left[a(n) \cdot e^{-j(\Delta\omega_M \cdot m)\cdot n} \right] = \sum_{n=0}^{M-1} \left[a(n) \cdot e^{-j\frac{2\pi \cdot m}{M} \cdot n} \right] \tag{2}$$

In the ROI Detector, the frequency index of interest m_r is selected. That is, the estimated coarse beat-frequency is determined according to $\Delta\omega_M \cdot m_r$. In this case, since the round-off error of the M-point FFT is K times greater than the N-point FFT, the radian frequencies between $\Delta\omega_N \cdot (n_r - K/2)$ and $\Delta\omega_N \cdot (n_r + (K/2) - 1)$ are mapped to the $\Delta\omega_M \cdot m_r$. Therefore, if the spectrum of $a(n)$ can be re-analyzed within the bound of these frequencies, we can obtain the frequency precision with the same value determined from N-point FFT.

Thus, in the paper, in order to estimate the high precision frequency from the coarse ROI frequency $\Delta\omega_M \cdot m_r$ we employ a frequency spectrum estimator consisting of a complex multiplier-accumulator. In the estimator, the fine frequency spectrum of $a(n)$ can be extracted by multiplying and summarizing the received signal $a(n)$ and $h_k \cdot (m_r, n)$ as shown in Eq. (3). The radian frequency of the complex sinusoid reference $h_k \cdot (m_r, n)$ is expressed as $\Delta\omega_N(K \cdot m_r - k)$ and k is the frequency index bounded by the coarse ROI, where $k = -K/2 \sim (K/2) - 1$.

$$\begin{aligned} Z_k &= \sum_{n=0}^{N-1} \left[a(n) \cdot h_k(m_r, n) \right] = \sum_{n=0}^{N-1} \left[a(n) \cdot e^{-j(\Delta\omega_M \cdot m_r - \Delta\omega_N \cdot k)\cdot n} \right] \\ &= \sum_{n=0}^{N-1} \left[a(n) \cdot e^{-j(\Delta\omega_N \cdot (K \cdot m_r - k))\cdot n} \right] \end{aligned} \tag{3}$$

Since the proposed FSE consists of an N-point multiplier, its time complexity is expressed as N. If

K time processing is carried out using a single frequency spectrum estimator, the total complexity is defined as $N \cdot K$. However, if several FSEs are employed for parallel processing, the time complexity can decrease as in $N \cdot K/L$, where L is the number of FSE processors implemented for parallel processing. Therefore, the whole time complexity of the proposed hardware architecture consisting of the N-point FFT engine and the N-point FSE processor can be expressed as $M \cdot \log M + (N \cdot K)/L$.

Figure 2 provides a time complexity comparison of the traditional full-point FFT and the proposed architecture, based on the number of samples (N). Both axes are plotted in log scale. In the case in which $K = 16$ and $L = 1$, the typical full-point FFT processing has rather lower computational complexity. In these two scenarios, with $K = 16$ and $L = 2$, and $K = 8$ and $L = 1$, the more processing time of the proposed architecture is consumed in cases with a smaller sample. However, in other cases, the time complexity of the proposed method is always lower than that of the full-point FFT processor.

3. IMPLEMENTATION

In this paper, a typical architecture using an N-point FFT processor and the proposed architecture consisting of the M-point FFT processor are implemented based on the Xilinx FPGA Spartan-6 with ISE 12.1. We implement the FFT processor based on the *Xilinx LogicCORE^{TM} IP Fast Fourier Transform 7.1* [6]. Moreover, the proposed frequency spectrum estimation processor is implemented using the *LogicCORE^{TM} IP Complex Multiplier 3.1* [7].

In order to analyze used hardware resource and required processing time, we design and implement two architectures. That is, in order to support a resource optimized approach, an FFT processor with a *Radix-2 Lite Burst IO* architecture and a single FSE processor are used. On the other hand, for the processing time enhanced architecture, a *Pipelined Streaming IO* FFT structure and a parallel FSE processing are employed.

In the two implementations, the total data number N is 4096 and the reduced FFT point M for the proposed architecture is selected to be 512. Therefore, the reduced ratio of FFT point K is 8. We also determined one FSE processor ($L = 1$) for the hardware resource minimized design and eight frequency spectrum estimators ($L = 8$) for the high speed parallel processing. Moreover, we assumed that all input and output data were aligned in terms of size at 16 bit.

Table 1: Hardware cost and latency of the typical and the proposed architecture.

Design mode	Processing architecture	Used hardware resources		Latency (clocks)
		Flipflops	Slices	
Resources optimized design	Typical method	1,711	964	57,377
	Proposed method (L=1)	1,538	704	38,433
Speed enhanced design	Typical method	11,032	3,404	8,326
	Proposed method (L=8)	8,538	3,208	5,230

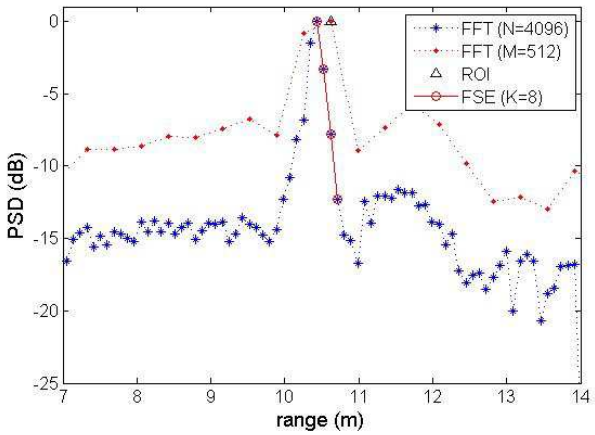

Figure 3: Range profile for target at about 11 m range.

As for implementation results from the synthesis tools with the default setting, the utilized hardware resources and the latency of the processing time are listed in Table 1. The table shows that the usages of Flipflops and Slices decreased in the proposed architecture. In particular, the processing clock is reduced by 33% and 37% in these two design modes, respectively.

Finally, the performance of the proposed architecture is estimated using a real 24 GHz FMCW radar module, developed by DGIST, as shown in Fig. 3. The x-axis is the range and the y-axis is the normalized PSD (Power Spectrum Density) with dB scale. The parameters for measurement are the same as those shown in the results in Table 1. These results show that the 4096-point FFT results and the results for the proposed architecture have an equal range profile around the ROI.

4. CONCLUSION

In this paper, we propose a high precision range measurement processor architecture for FMCW radar systems. The proposed architecture consists of an FFT processor with a reduced point and a frequency spectrum estimation processor based on a complex multiplier-accumulator. In the implemented results, the proposed architecture can reduce the utilized hardware resources by an average of 15% and the processing time by up to 30% compared with those values for the traditional method. Moreover, according to the experiment results, the range precision of the proposed architecture is the same as that of the typical method based on full-point FFT processing. Therefore, the proposed range measurement radar can be expected to be useful for level gauging systems with competitive prices.

ACKNOWLEDGMENT

This work was supported by the DGIST R&D Program of the Ministry of Science, ICT and Technology of Korea (15-RS-01).

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