Low-complexity Design of an 8×8 Modulation Configurable K-best MIMO Detector

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Abstract— In this paper, a low complexity 8×8 MIMO detector supporting QPSK, 16-QAM, and 64-QAM is presented. A breadth-first type known as distributed K-best (DKB) algorithm is applied in the design. Compared with the conventional K-best algorithm, the DKB reduces the number of visited nodes at each layer from $K\sqrt{M}$ to $2K-1$, where K and M are the quantity of candidates and constellation size, respectively. To further reduce power consumption, a shift multiplier which simply operates bits shifting and additions is proposed to replace the conventional multiplier. In addition, the proposed multi-stage circuit architecture only requires K clock cycles to find the best K candidates, and the sorting circuits for the conventional K-best can be avoided in our design. The proposed 8×8 MIMO detector has been implemented by a 90-nm CMOS technology with a core area of $0.99 \times 0.99\,\mathrm{mm}^2$. The average power consumption is about 17.2 mW at 74 MHz and 1 V supply voltage.

1. INTRODUCTION

Multiple-input multiple-output (MIMO) technologies have become a trend in the recent communication standards to enhance the channel capacity and signal reliability. From standpoint of improving bandwidth efficiency, *Spatial multiplexing* is the most studied MIMO technique, which can effectively increase the data throughput within a limited bandwidth. Let us consider a spatial multiplexing MIMO system with N_t transmitter antenna and N_r receiver antenna. The real-valued baseband equivalent model can be written as:

$$\mathbf{Y} = \mathbf{Hs} + \mathbf{n}. \tag{1}$$

In (1), $\mathbf{s} = [\Re\{s_1\, s_2 \ldots s_{N_t}\}\, \Im\{s_1\, s_2 \ldots s_{N_t}\}]^T$ is the transmitted symbol vector. For each element s_i is independently chosen from M-QAM constellation set Ω and transmitted by ith antenna, where $\Re\{\cdot\}$, $\Im\{\cdot\}$ and $[\cdot]^T$ imply taking real and imaginary part of a signal and transposing of a matrix; $\mathbf{Y} = [\Re\{y_1\, y_2 \ldots y_{N_r}\}\, \Im\{y_1\, y_2 \ldots y_{N_r}\}]^T$ is the received symbol vector by N_r antennas; $\mathbf{H}$ denotes the real-valued channel matrix of size $2N_r \times 2N_t$, whose entries are identically independent distributed (i.i.d) zero-mean Gaussian random variables; and $\mathbf{n} = [n_1\, n_2 \ldots n_{2N_r}]^T$ is a white Gaussian noise vector with variance $\frac{\sigma^2}{2}$. The optimum solution for (1) is called maximum-likelihood (ML) decoding, which finds out the most likely symbol vector $\hat{\mathbf{s}}$ according to minimum-distance criterion as follows:

$$\hat{\mathbf{s}} = \arg\min_{\mathbf{s} \in \Omega^{2N_t}} \|\mathbf{Y} - \mathbf{Hs}\|^2. \tag{2}$$

The ML decoder should exhaustively compute $\sqrt{M}^{2N_t}$ possible symbol vectors to determine one $\hat{\mathbf{s}}$. Its complexity grows exponentially with the number of antenna and constellation order. Thus, such ML decoder is not feasible for hardware implementation.

Consequently, some simplified recursive searching algorithms have been developed for practical realization. According to the searching direction, these approaches can be classified into two categories, the *depth-first* type and *breadth-first* type [1]. Compared with depth-first algorithm, K-best belonged to the breadth-first algorithm is suitable for a high throughput MIMO detector design. Because K-best owns forward tree-searching path and regular path pruning rule, it can be implemented in a paralleled pipelined fashion. Several researches have investigated the MIMO detection based on K-best algorithm [1–4]. However, most of these published studies only provide 4×4 antenna configuration and cannot support multiple modulation schemes.

To transforming ML decoding into tree-branch searching, thanks to QR decomposition, i.e., $\mathbf{H} = \mathbf{QR}$, where $\mathbf{R}$ and $\mathbf{Q}$ are upper triangle matrix and unitary matrices, respectively. By applying $\mathbf{Q}^H$ at both left and right sides of (1), results in $\tilde{\mathbf{Y}} = \mathbf{Q}^H\mathbf{Y} = \mathbf{Rs} + \mathbf{Q}^H\mathbf{n} = \mathbf{Rs} + \mathbf{w}$.

Since $\mathbf{R}$ is an upper triangular matrix, (2) can be re written in recursive form by above formula:

$$\hat{\mathbf{s}} = \arg\min_{\mathbf{s}\in\Omega^{2N_t}} \sum_{i=1}^{2N_r} \underbrace{\left| \tilde{y}_i - \sum_{j=i}^{2N_t} R_{ij} s_j \right|^2}_{i\text{th layer PED: } e_i(s^{(i)})} . \tag{3}$$

The tree-searching process starts from layer-$2N_t$ down to layer-1 and calculates accumulated *partial Euclidean distance* (PED): $T_i(s^{(i)}) = T_{i+1}(s^{(i+1)}) + e_i(s^{(i)})$ at ith layer to find the best path which owns minimum PED in (3).

The conventional K-best scheme can concurrently expand and sort the children nodes to find the candidates. However, the best K candidates of DKB scheme are one by one sequentially listed in $\mathbf{K}_i$ within K clock cycles. Owning to this feature, the DKB can avoid the complicated sorting circuit and only requires a minimum finder circuit to select the child in $\mathbf{L}_i$ which has minimum PED. It should be noted that the number of visited nodes at each layer is $2K-1$, which is independent of the constellation size M. Therefore, the DKB is more suitable to apply to expand to high-order constellation modulations. The total number of visited nodes for DKB is $\sqrt{M}+(2N_t-1)(2K-1)$. Compared to the conventional K-best algorithm, the DKB scheme is a efficient procedure to choose the best K candidates.

In this paper, the 8×8 MIMO detector which can flexibly support various modulation schemes, such as QPSK, 16-QAM and 64-QAM, is presented. Besides, the proposed detector also supports unequal modulation, i.e., different spatial streams can apply unequal modulation schemes. In our design, we adopt a modified K-best algorithm with lower computational complexity to save power consumption. In addition, a novel shift multiplier (SM) is proposed to simplify the multiplication complexity.

2. ARCHITECTURE AND CIRCUIT DESIGN

The architecture of the proposed multi-stage 8×8 MIMO detector is depicted in Fig. 1. The DKB building block consists of a *first child unit* (FCU), a *next child unit* (NCU) and register banks. The register banks are used to store the PEDs, the contender list $\mathbf{L}_i$ and the K-best candidate list $\mathbf{K}_i$ at i-th layer. According to the K-best candidates result $\mathbf{K}_{i+1}$ from the previous layer, in the first, the FCU finds out the corresponding K FCs and stores them into the contender register. Their PEDs are also stored into the PED register. As all the K PEDs have been computed by the FCU, the NCU will find the minimum PED index and select the corresponding FC into the K-best candidate register $\mathbf{K}_i$. Meanwhile, the NCU enumerates its best sibling node as the next child (NC). Then the selected FC in contender register $\mathbf{L}_i$ is replaced by this NC and the PED register is also updated with this NC PED. In each cycle, the FCU and NCU can determine one FC and NC, respectively. Therefore, each DKB stage completes the best K candidates and delivers them to the next pipelined stage within K clock cycles. An advantage of this DKB pipeline architecture is that the K-value can be configured flexibly due to its regular hardware manner.

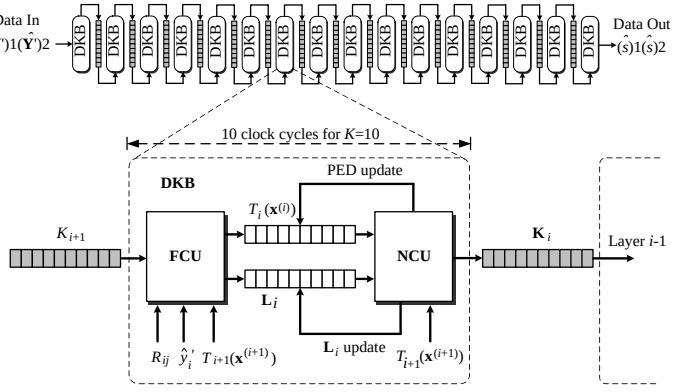
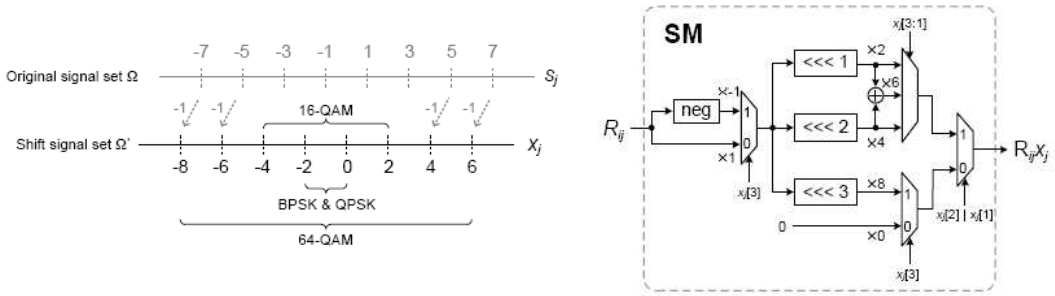


Figure 1: Circuit architecture of the proposed multi-stage 8×8 MIMO detector.

2.1. Shift Multiplier

From (3), it can be seen that the multiplication of R_{ij} and s_j play the most complicated roles in the PED computation. In order to simplify the multiplication complexity, we propose a *shift multiplier* (SM) approach which can reduce the area and critical path delay of the multiplication significantly. In convention, $s_j \in \Omega = \{-\sqrt{M}+1, \ldots, -1, 1, \ldots, \sqrt{M}+1\}$ is an odd number set in the real-valued axis, and $R_{ij}s_j$ requires a real multiplier. The SM approach uses a new signal set $\Omega' = \{-\sqrt{M}, \ldots, -2, 0, \ldots, \sqrt{M}\}$ instead of Ω by left shifting the original axis by one. The new signal set Ω' is represented in Fig. 2(a). In the case of 16-QAM, each value of new signal set is power of two, i.e., $\Omega' = \{-4, -2, 0, 4\}$.



(a) Representation of the shifted signal set (b) Circuit diagram of the shift multiplier

Figure 2: (a) Representation of the shifted axis. (b) Hardware implementation of the shift multiplier.

Therefore, R_{ij} multiplied by the shifted signal can be implemented by the proposed SM circuit. The received signal vector $\hat{\mathbf{Y}}$ can be represented by:

$$\hat{\mathbf{Y}} = \mathbf{R}(\mathbf{s} - \mathbf{e}) + \mathbf{R}\mathbf{e} + \mathbf{w}, \tag{4}$$

where $\mathbf{e} = [1\,1\,\ldots\,1]^T$ is a $2N_t \times 1$ all one vector. Let $\mathbf{x} = \mathbf{s} - \mathbf{e}$ be the new shifted signal vector in set Ω'. Then (4) can be rewritten as:

$$\hat{\mathbf{Y}}' = \hat{\mathbf{Y}} - \mathbf{R}\mathbf{e} = \mathbf{R}\mathbf{x} + \mathbf{w}. \tag{5}$$

The decoding process of (5) is identical to the (2) except the new shifted signal $\mathbf{x}$ and the new received vector $\hat{\mathbf{Y}}'$

Since our design supports multiple modulation schemes from QPSK to 64-QAM, the new maximum range of signal set $x_j \in \Omega' = \{-8, -6, -4, -2, 0, 2, 4\}$ should be considered. R_{ij} multiplied by values $(\pm 2, \pm 4, 8)$ is realized by only shift operation. The computation of $\pm 6R_{ij}$ can also be easily implemented by $(\pm 2R_{ij}, \pm 4R_{ij})$ with summation. The block diagram of the proposed SM circuit is depicted in Fig. 2(b). The "neg" block denotes the sign inversion operation.

2.2. FCU and Configurable NCU

For each parent node in $\mathbf{K}_{i+1}$, the FCU of the i-th layer is used to find the FC with the smallest PED. Eq. (3) shows that the FC of a parent node in $\mathbf{K}_{i+1}$ is the one which has the minimum distance increment $|e_i(\mathbf{x}^{(i)})|^2$, i.e.,

$$x_{i,\mathrm{FC}} = \arg\min_{x_i \in \Omega'} \left| \underbrace{\hat{y}'_i - \sum_{j=i+1}^{2N_t} R_{ij}x_j}_{\text{center } C_i(\mathbf{x}^{(i)})} - R_{ii}x_i \right|^2, \tag{6}$$

where $C_i(\mathbf{x}^{(i)})$ is referred to as *center*. Thus the FC can be found by quantizing $C_i(\mathbf{x}^{(i)})/R_{ii}$ to the nearest constellation signal in Ω'.

When the FC is decided, the NC that belongs the same parent node can be enumerated based on zigzag principle. The zigzag operation of 1D SE-enumeration for 16-QAM is given in Fig. 3(a).

The l-th enumeration of NC can be expressed as follow:

$$\begin{aligned} \mathrm{NC}(l+1) &= \mathrm{NC}(l) + d(l) \times \mu(l) \\ \mu(l+1) &= \mu(l) + 2 \\ d(l+1) &= \begin{cases} -d(l), & \text{if BoundFlag} = 0 \\ d(l), & \text{if BoundFlag} = 1, \end{cases} \end{aligned} \tag{7}$$

where l starts at zero and NC(0)=FC; $d(l)$ denotes right or left enumerative direction, and $d(0) = +1$ or -1 depends on the center falling on right or left side of the FC; μ is the enumerative step-size and $\mu(0) = 2$. The step-size is accumulated by two after each enumeration. Since there are K FC candidates that may enumerate their NCs, we need to record three current statues of the K NCs for the next enumeration. The three status are enumeration direction, step-size and NC value. The enumeration circuit diagrams are shown in Fig. 3(b). In each clock cycle, the step-size with "MinIdx" is accumulated by two and change direction by multiplying (± 1). The the *MinIdx*-th NC can be enumerated according to (7).

2.3. Chip Implementation and Comparison

The proposed 8×8 MIMO detector is implemented in 90-nm CMOS technology. The core area of this chip is $0.99 \times 0.99\,\mathrm{mm}^2$ and the power consumption is 17.2 mW operating at 74 MHz and 1 V supply voltage. The throughput of this design is given by $\Phi = (N_t \log_2 M) f_{\mathrm{clk}}/K$, where f_{clk} is the clock frequency. Since our design supports two K-value configurations, i.e., $K = 5$, 10, this

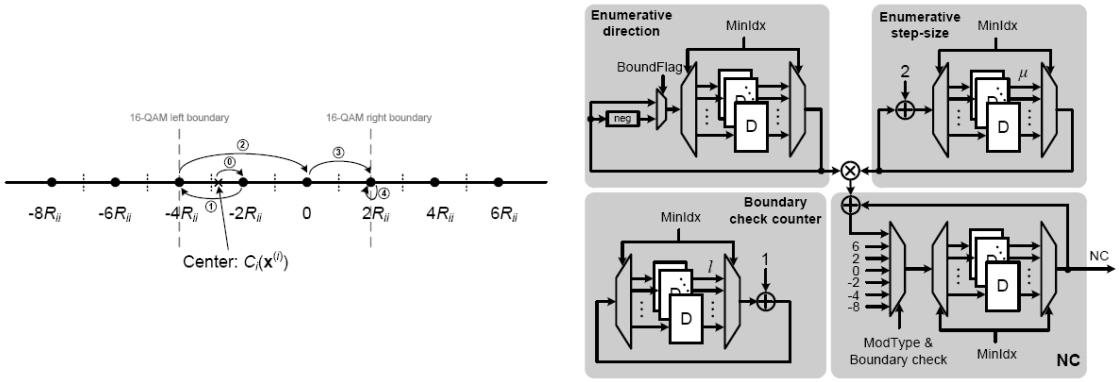


Figure 3: (a)Representation of the 1D SE-enumeration for 16-QAM. (b) Circuit diagram of the configurable NC enumeration.

Table 1: Chip comparison of the MIMO detectors.

Reference design	JSAC' 06 [1] IC1	JSSC' 05 [6]	TVLSI' 07 [4]	ISSCC' 09 [7]	JSSC' 10 [8]	This work	
Antenna	4×4	4×4	4×4	4×4	$N_t = 2 \sim 8$ $N_r = 2 \sim 8$	8×8	
Modulation	16-QAM	16-QAM	64-QAM	64-QAM	QPSK 16-QAM 64-QAM	QPSK 16-QAM 64-QAM	
Algorithm	K-best	Depth-first	K-best	DKB	MBF-FD	DKB	
Model (Real/Complex)	Real	Complex	Complex	Real	Complex	Real	
Output type	Hard	Hard	Soft	Hard	Soft	Hard	
Technology	0.35 μm	0.25 μm	0.13 μm	0.13 μm	0.13 μm	0.09 μm	
Gate count	91 K	117 K	280 K	114 K	350 K	323 K	
Area (mm^2)	5.76	N/A	2.38	2.31	1.77	0.98	
Max. clock rate	100 MHz	51 MHz	270 MHz	282 MHz	198 MHz	74 MHz	
Max. throughput (Mbps)	53.5	73.5	8.57	675	429 (88, 64-QAM)	*K*=5 710	*K*=10 355
Power (mW)	626	360	94	135	74.8	17.15	17.2
Normalized power (pJ/bit)	384 (7.28%)	282 (5.35%)	5273 (100%)	82 (1.55%)	71 (1.35%)	24 (0.46%)	49 (0.92%)

chip can provide a maximum throughput at 710 Mbps. Table 1 lists the performance comparison between this chip and other MIMO detector ICs. To eliminate the process factor, the normalized power is formulated as

$$P_{\text{norm}} = \text{power} \times \left(\frac{1.0}{V_{\text{dd}}}\right) \times \left(\frac{0.09}{\text{Tech}}\right) \times \left(\frac{1}{\text{Throughput}}\right).$$

From Table 1, our design consumes less power and has high power efficiency than other listed ICs.

3. CONCLUSION

In this paper, we have presented a low-complexity design of 8×8 modulation configurable MIMO detector. From the algorithmic aspect, the DKB scheme provides efficient candidate searching procedure. In terms of hardware design, the new signal set Ω' allows the SM to replace the conventional complicated multiplier. Furthermore, multiple modulation schemes from QPSK to 64-QAM are flexibly supported in our design. This chip is implemented in 90-nm CMOS technology and achieve significant improvement in power consumption by low complexity hardware design.

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