Analog Multiplexer with an Improved High Linearity Bootstrapped Switch for Multi-channel Neural Signal Recording

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Abstract— An analog integrated multiplexer and a bootstrapped switch for the interface of multi-channel neural signal recording system is presented. The bootstrapped switch is improved to suit the specific environment, which satisfies the requirements of constant clock feed-through, constant charge injection, and compensation for body-effect Simulation results show a higher linearity comparing the proposed switch with the conventional bootstrapped switches. Under typical-case conditions the switch maintains about −107 dB THD for an input signal with the frequency range of 1 kHz∼10 kHz.

1. INTRODUCTION

The acquisition of neural signals has received significant interest from the neuroscience research community very recently, as it has been thought that neural signals can be the key to study functional mapping of the brain. The advent of micro-electrode arrays acquiring electric signals from neurons has driven the need for electronics which is used to amplify, filter, and digitize neural signals. Since the number of the electrodes should be affirmatively much larger than the number of recording channels, the multiplexer is necessary in such systems. Taking into account our special application, the multiplexer here is expected to have the following characteristics:

- High linearity.
- Low power consumption.
- Low noise.

Meanwhile, another important requirement in many systems where analog multiplexer are used is for the ON resistance of the closed switch to remain constant when either or both the analog input and the supply voltages change. The ON resistance of a MOS transistor when used as a switch changes with variations in the amplitude of the analog signal and the supply voltages.

This paper is organized as follows: Section 2 presents a description on the structure of the multiplexer. In Section 3, certain issues related with the design of bootstrapped switch are introduced and an improved high linearity bootstrapped switch for multi-channel neural signal recording is presented. Simulation results are shown in Section 4. Finally, conclusions are drawn in Section 5.

2. MULTIPLEXER ARCHITECTURE

An analog integrated multiplexer is an indispensable element for the input analog interface of multi-channel neural signal recording system. The block diagram of the analogue multiplexer is shown in Fig. 1.

The multiplexer contains N input channels and an extra channel which is added as a reference to cancel the offset and the cross-talk. Each channel consists of hold switch, sample switch, a storage capacitor and necessary buffers. The multiplexing function is implemented by a simple array of hold and sample switches controlled by a control module.

3. SWITCH DESIGN

Considerable attention is paid to low distortion performance of the multiplexer as it is the importance part delivering the amplified neural signals to the analog to digital converters. However, most switches in multiplexers suffer from the distortion of passing signals from the non-ideality of the MOS transistor [1].

3.1. Non-linearity Source of the MOSFET Switch

The following are some effects producing deviation which degrading the linearity and the resolution:

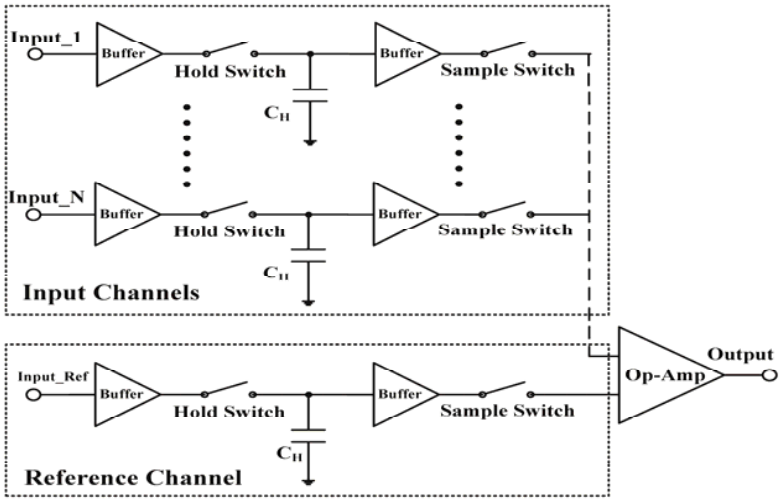

Figure 1: Block diagram of analogue multiplexer.

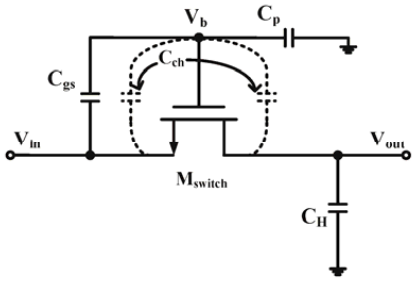

Figure 2: The model of a MOSFET switch.

3.1.1. Threshold Voltage Variation

A CMOS transistor used as a switch has a non-zero on-resistance. The on-resistance can be approximated as:

$$R_{on} = \frac{\partial V_{ds}}{\partial I_d} = \frac{1}{\mu C_{ox} \frac{W}{L} (V_{gs} - V_{TH} - V_{ds})} \tag{1}$$

This means that the on-resistance becomes signal dependent.

3.1.2. The Parasitic Capacitance

As Fig. 2 shows, both the generation of the inverter layer under the gate and the total equivalent capacitance C_{gs} (the sum of all capacitance between gate-source), C_p (the parasitic capacitance between the gate-ground) will significantly reduce the gate voltage. This charge leakage effect can be formulated by:

$$V_{gs} = \frac{C_{gs}}{C_{gs} + C_{ch} + C_p} V_b - \frac{C_p}{C_{gs} + C_{ch} + C_p} V_{in} \tag{2}$$

V_{gs} is the practical voltage between the gate and source. C_{ch} is the equivalent capacitance of the inverter layer.

3.1.3. Charge Injection

The charge that has been build up in inverter layer of the channel will be divided between the source and drain side when a transistor turns off. In the worst case, all the charges are injected into the output node which is approximated with Formula (3):

$$\Delta V_{ci} = \frac{WLC_{ox}}{C_H} (V_{gs} - V_{TH}) \tag{3}$$

Here, C_H is the total capacitance on the output terminal.

3.1.4. Clock Feed-through

The parasitic capacitance between the gate-source or gate-drain will feed-through the clock signal to the output node which can be approximated as:

$$\Delta V_{cf} = (V_{gs,on} - V_{gs,off}) \frac{C_g d}{C_{gd} + C_H} \tag{4}$$

3.2. Bootstrapped Switch

Bootstrapped switch is attractive as a circuit technique to deal with the aforementioned non-linearity sources which is widely employed for low-voltage, high-linearity applications [2–12]. The main idea behind this technique is to keep the gate-to-source voltage of a transistor constant to be constant. A high linearity bootstrapped switch is proposed here which is improved in body effect, charge leakage, charge injection and clock feed-through. As shown in Fig. 3, the proposed bootstrapped switch works on two phases in which the M_{sw} is turned on and off.

3.2.1. Phase "off" ($\boldsymbol{\varphi_2}$)

During the phase "off", the M_{sw} is turned off. The two capacitors C_{b1} and C_{b2} are charged by a pair of complementary power supply V_{DD} and V_{SS}. The M_{n2} controlled by gate-voltage $\overline{CLK}$ and M_{p4} by CLK connect the C_{b1} to V_{SS} and V_{DD}. Simultaneously, M_{p6} with the gate-voltage CLK clamps the gate-voltage of M_{p3} to V_{DD} and keeps it in "off" state which isolates the drain of M_{p4} from V_{SS}. Both M_{p3} and M_{n1} are in off-state during this phase. Analogously, C_{b2} is connected to V_{DD} and V_{SS} by M_{p8} and M_{p10} which are in on-state. At the end of this phase, the gate voltage of M_{sw} is pre-set on a low input-dependent level by a path composed of M_{n13} and M_{n15} to keep the clock feed-through a constant throughout the switching period of φ_2 to φ_1.

3.2.2. Phase "on" ($\boldsymbol{\varphi_1}$)

During the phase "on", the CLK goes high and M_{n9} is excited to be on-state which provide a path for the charged capacitor C_{b1} acting as a battery to pump charge onto the gate of M_{sw}. The increased gate-voltage turns on the M_{sw} and M_{n1}. Specifically, the voltage across the gate and source of the M_{sw} is a constant offset setting by C_{b1} regardless of the variable input signal. Moreover, M_{n5} and M_{n7} provide a path for C_{b2} to compensate the threshold voltage variation and eliminate the non-linearity of body effect.

4. RESULTS

The switch is simulated in the 0.5 µm CMOS technology using BSIM3v3 device model. The transistor level simulations are done in Cadence Virtuoso Analog Design Environment. The dynamic performance of the bootstrapped switch is depicted in Fig. 5. The results for HD2 and HD3 are illustrated in Fig. 6.

As Table 1 shows, some design of bootstrapped switches presented by other articles are compared with the one proposed here. The calculations of total harmonic distortion were carried out by

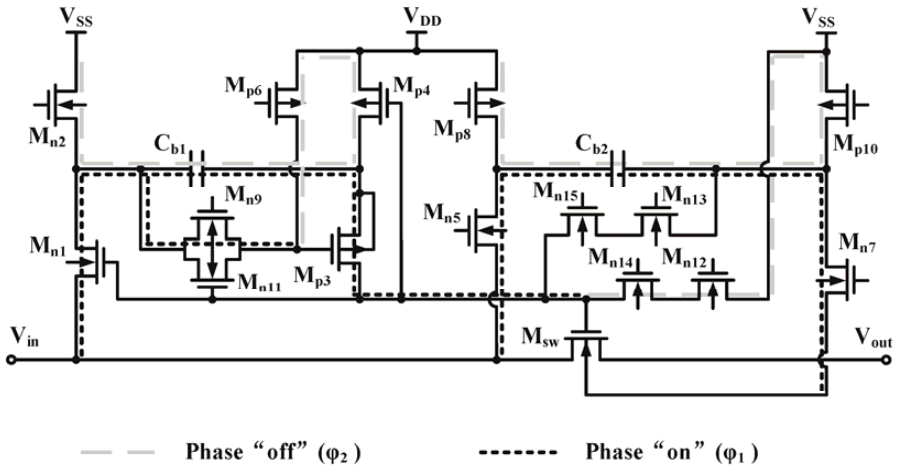

Figure 3: The schematic of the proposed bootstrapped switch.

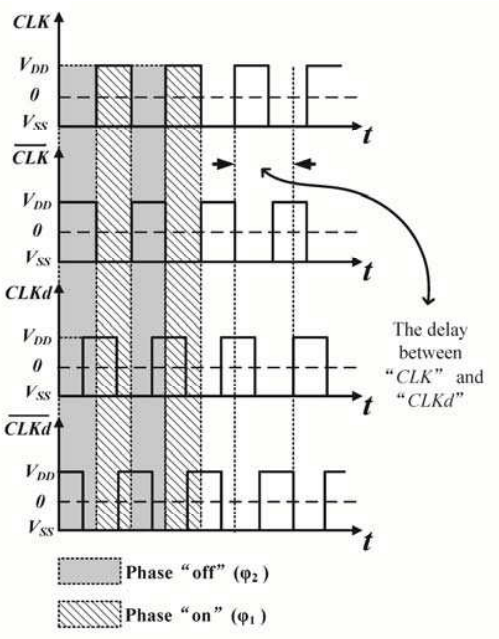

Figure 4: Time-domain switching scheme for the operation of the proposed bootstrapped switch.

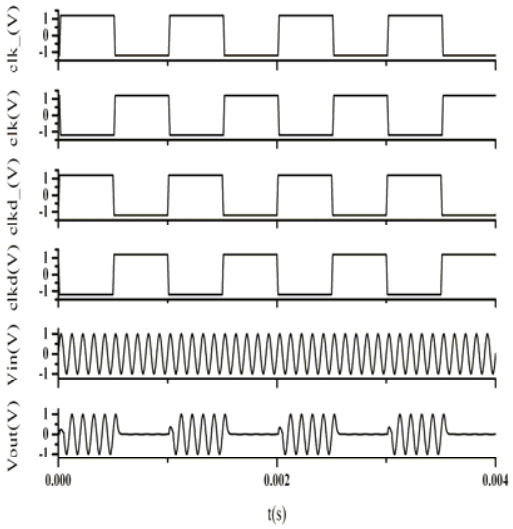

Figure 5: Simulated switch behavior with a dynamically changing input signal.

Table 1: Comparison of the harmonic distortion.

	THD	THD2	THD3
Conventional @ $f_s = 100\,\text{MHz}$	$-85.3\,\text{dB}$	$-85.2\,\text{dB}$	$-106\,\text{dB}$
Ref. [8] @ $f_s = 300\,\text{MHz}$	$-84.1\,\text{dB}$	$-87.9\,\text{dB}$	$-105.9\,\text{dB}$
Ref. [10] @ $f_s = 100\,\text{MHz}$	$-101\,\text{dB}$	$-102\,\text{dB}$	$-115.4\,\text{dB}$
Ref. [12] @ $f_s = 125\,\text{MHz}$	$-105\,\text{dB}$	$-110\,\text{dB}$	$-115\,\text{dB}$
Proposed @ $f_s = 10\,\text{MHz}$	$-107\,\text{dB}$	$-113\,\text{dB}$	$-116\,\text{dB}$

using the calculator option "THD" of Cadence Analog Design Environment. The range of values of input signal frequencies was from 1 kHz to 10 kHz.

5. CONCLUSIONS

In this article, a bootstrapped switch is proposed which has improvement in the requirements of constant clock feed-through, constant charge injection, and compensation for body-effect. Meanwhile, the switch remains the practicability for less increase in complexity. An exemplary 4-channels analog multiplexer is constructed based on the proposed bootstrapped switch for verifying the effectiveness of the optimization. As the simulation results show, a higher linearity comparing with the switch in other work is achieved in the proposed bootstrapped switches.

ACKNOWLEDGMENT

This work is sponsored by NUPTSF (NY214124).

REFERENCES

1. Razavi, B., *Design of Analog CMOS Integrated Circuits*, 1st Edition, McGraw-Hill, 2000.
2. Abo, A. M. and P. R. Gray, "A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter," *IEEE J. Solid-State Circuits*, Vol. 34, No. 5, 599–606, May 1999.
3. Dessouky, M. and A. Kaiser, "Input switch configuration suitable for rail-to-rail operation of switched-opamp circuits," *Electron. Lett.*, Vol. 35, No. 1, 8–10, Jan. 1999.
4. Steensgaard, J., "Bootstrapped low-voltage analog switches," *Proc. ISCAS*, Vol. 2, 1129–1132, 1999.
5. Waltari, M. and K. Halonen, "Bootstrapped switch without bulk effect in standard CMOS technology," *Electron. Lett.*, Vol. 38, No. 12, 555–557, 2002.

6. Dessouky, M. and A. Kaiser, "Very low-voltage digital audio modulator with 88-dB dynamic range using local switch bootstrapping," *IEEE Journal Solid-State Circuits*, Vol. 36, No. 3, 349–355, Mar. 2001.
7. Fayomi, C. J. B., G. W. Roberts, and M. Sawan, "Low-voltage CMOS analog bootstrapped switch for sample-and-hold circuit: Design and chip characterization," *Proc. IEEE Int. Symp. on Circuits and Systems*, Vol. 3, 2200–2203, May 2005.
8. Yang, C. Y. and C. C. Hung, "A low-voltage low-distortion MOS sampling switch," *Proc. IEEE Int. Symp. on Circuits and Systems*, Vol. 4, 3131–3134, May 2005.
9. Cornelissens, K. and M. Steyaert, "A novel bootstrapped switch design, applied in a 400 MHz clocked $\Delta\Sigma$ ADC," *13th IEEE International Conference on Electronics, Circuits and Systems, ICECS'06*, 1156–1159, 2006.
10. Wang, L., J. Ren, W. Yin, T. Chen, and J. Xu, "A high-speed high-resolution low-distortion CMOS bootstrapped switch," *IEEE ISCAS 2007*, 1721–1724, May 2007.
11. Pan, H., et al., "A 3.3-v 12-b 50-MS/s A/D converter in 0.6-μm CMOS with over 80-dB SFDR," *IEEE JSSC*, Vol. 35, No. 12, 1769–1780, Dec. 2000.
12. Chen, H., L. He, et al., "A high-performance bootstrap switch for low voltage switched-capacitor circuits," *2014 IEEE International Symposium on Radio-Frequency Integration Technology (RFIT)*, 1–3, 2014.