Low Power Dissipation SEU-hardened CMOS Latch

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Abstract—This paper reports three design improvements for CMOS latches hardened against single event upset (SEU) based on three memory cells appeared in recent years. The improvement drastically reduces static power dissipation, reduces the number of transistors required in the VLSI, especially when they are used in the Gate Array. The original cells and the new improved latches are compared. It is shown that the new latch-NDICE latch has the best composite capability and the best SEU immunity.

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1. INTRODUCTION
To ensure the reliability of electronic systems in space, electronic circuitry must be resilient when exposed to the radiant space. The effects of the single event (SEE) have become more critical as clocks speeds have increased and feature sizes have decreased in modern IC processes. The main SEE includes SEU and single event latch (SET). SEU phenomenon may result in the corruption of data in memory cells and in the propagation of erroneous signals in combinational logic circuits. As a result, it is increasingly clear that hardening approaches for both combinational logic and memory elements are needed.

In recent years, there have been many designed SEU-Hardened CMOS memory cells which were designed by Rockett, Whitaker, Liu respectively and the HIT [1–5], DICE [6], DICE with Guard-gates [7]. Through [5] we know that the HIT is better than the pioneering three SEU-hardened memory cells. But the original HIT, DICE and DICE with Guard-gates have their advantages and disadvantages respectively.

The combinational logic and memory elements are mainly from latch, so this paper reports three SEU-Hardened CMOS latches considering of their static power dissipation and the number of the transistors synthetically. The three latches in the paper are mainly improved from the HIT, DICE and DICE with Guard-gates respectively. The results make them have lower static power dissipation and fewer transistors.

In Section 2, the design method, functionality and performance of the proposed SEU-hardened latches are described. Section 3 compares the improved latches with the original cells [5–7].

2. LATCH DESIGN
The three original cells used to design the SEU-hardened latches are shown in Figures 1, 2 and 3 respectively.
2.1. The HIT Cell

The HIT cell is composed of 12 transistors organized as two storage structures interconnected by feedback paths. The read/write operation needs a single phase clock CK and differential input D and DN. The output Q and its complement QN are both available.

It has three sensitive notes: Q, QN, A/B. If a particle strikes the drain of transistor to make only one sensitive node to upset, it can recover quickly. But if both nodes upset, the contents of the memory cell will be corrupted. To cope with single upset, specific transistors ratios have been used (Table 1).

But our aim is to use the cell in gate array. So the transistors must be in the same size. In order to make it suitable for our demand, we connect one PMOS transistor in parallel with P5 and P6 respectively.

<table>
<thead>
<tr>
<th>Transistors</th>
<th>Wn(µm)</th>
<th>Ln(µm)</th>
<th>Transistors</th>
<th>Wp(µm)</th>
<th>Lp(µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>N1</td>
<td>6.0</td>
<td>1.2</td>
<td>P1</td>
<td>8.0</td>
<td>1.2</td>
</tr>
<tr>
<td>N2</td>
<td>6.0</td>
<td>1.2</td>
<td>P2</td>
<td>8.0</td>
<td>1.2</td>
</tr>
<tr>
<td>N3</td>
<td>6.0</td>
<td>1.2</td>
<td>P3</td>
<td>4.0</td>
<td>1.2</td>
</tr>
<tr>
<td>N4</td>
<td>6.0</td>
<td>1.2</td>
<td>P4</td>
<td>4.0</td>
<td>1.2</td>
</tr>
<tr>
<td>N5</td>
<td>6.0</td>
<td>1.2</td>
<td>P5</td>
<td>6.0</td>
<td>1.2</td>
</tr>
<tr>
<td>N6</td>
<td>6.0</td>
<td>1.2</td>
<td>P6</td>
<td>6.0</td>
<td>1.2</td>
</tr>
</tbody>
</table>

All the transistors of the new HIT latch are the same size, none is special. Though it has two more PMOS transistors, there is no extra pre-existing word line driver needed, no matter what it is connected in the front. Also the parallel-connection make the part of P5 and P6 stronger than the P3 and P4. If a particle strikes the drain of transistor which is controlling the sensitive note: Q, QN, A/B, it can recover its initial state all. But it will lead to corruption of the data stored if both were stricken. There is no extra static power dissipation. In addition, the total dose effect is considered.
2.2. The DICE

The original DICE (Figure 2) puts no particular constraints on transistor sizes and it does not evidence the high sensitivity to total dose of the ration designs. Though it has four sensitive nodes: Q1, Q2, Q3 and Q4, the recovery process is very fast (much less than 1ns). It will lead to corruption of the data stored if both were stricken. But it requires two pre-existing word line drivers and hence a small increase in the dynamic power dissipation. Additional design changes are required to adapt the word line routing, the write buffer drive capability and column pass gate width to the increased load requirements.

To overcome these limitations the new improved DICE latch is developed. In order to reduce the write transistor, take out N71 and N81. Connect PMOS transistor P51 and P61 in parallel with N51 and N61 respectively, it will reduce the static power dissipation and the loss of threshold. Connect P12, N12 with P11 and N11 respectively in series, connect P22, N22 with P21 and N21 respectively. It can prevent the write state from the strife of the stored state. So it will reduce the pre-existing word line driver. There is no extra pre-existing word line drive needed, no matter what it connects in the front. So the P6, N6, P7, N7, P8, and N8 are all taken out. There is only P1 and N1 needed. For the dual interlocked structure, it presents excellent SEU immunity.

2.3. The Guard-gates DICE

The radiation performance for the guard-gates DICE (Figure 3) is better than DICE, because the only way to upset these cells with ion hits is by depositing charges on at least three of the storage nodes — an extremely low probability event. The proposed design isolates the gate outputs during a strike to preserve the data. As a result, it provides better protection against multiple node hits than regular DICE design. The write time will be improved because the feedback loop within the latch is disconnected. Additionally, in the presence of a single-event hit, DICE latches are subjected to short circuit current because p- and n-channel devices within an inverter will turn on simultaneously creating a short circuit between supply voltage and ground. This facilitates the upset by changing the output node voltage away from the supply rails. The guard-gate based designs avoid such a short circuit by disconnecting the output from the power supply and ground during the presence of an SET.

But the total number of transistors in the four guard-gates DICE is twice as that for a conventional DICE latch. In order to reduce the number of the transistor and the static power dissipation, use the same principle as the New DICE latch, we get the new improved Guard-gates DICE latch.

3. COMPARISON AND SPICE SIMULATION

Table 2 and Table 3 show some performance comparisons between the three original memory cells and the three new improved latches. HIT, DICE and GDICE stand for the original HIT, DICE and Guard-gates DICE cells respectively. NHIT, NDICE and NGDICE stand for the new HIT latch, DICE latch and Guard-gates DICE latch.

<table>
<thead>
<tr>
<th>Original cell</th>
<th>Power</th>
<th>N.PMOS</th>
<th>N.NMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>HIT</td>
<td>$2.2689 \times 10^{-5}$ W</td>
<td>12</td>
<td>12</td>
</tr>
<tr>
<td>DICE</td>
<td>$6.6599 \times 10^{-5}$ W</td>
<td>12</td>
<td>16</td>
</tr>
<tr>
<td>GDICE</td>
<td>$2.1262 \times 10^{-5}$ W</td>
<td>14</td>
<td>18</td>
</tr>
</tbody>
</table>

From Table 2, we can’t know the best cell. That is to say, the original cells have their own disadvantage and advantage. Through our improvement, all the power become smaller. Also we can see the best one is the NDICE which has the fewest transistors and least Power dissipation. The delay time is smaller.

For the sake of the SEU immunity of the latches, we design a single event transient model (Figure 4) to simulate the SEU. VCC is reduced from 1.8 V to 0 for 0.18 µm.

In the SPICE simulator, the heavy ion effect is modeled by injecting a hit current pulse at the sensitive note. This current pulse is of a rough triangular shape with rise time equal to 30 ps, rise and fall damping factor equal to 10 ps and 200 ps. The injection node is clamped to either GND or VCC by a variable current during charge collection. The method assumes the hit pulse is much...
faster than the circuit response and ignores the detailed timing information carried in the pulse shape. It is the-worse-case-design simulation to generate a relatively conservation critical charge for SEU. In the model, the I2 is variable. From Figure 5 we can get that $b = 1 \text{ mA}$ cause $Q_{\text{crit}} = 0.02 \text{ PC}$.

Make use of the conclusion in [8], we know for the most sensitive node, the crit $Q_{\text{crit}}$ to cause a propagating pulse is $0.02 \text{ PC}$ and the threshold LET is $2 \text{ MeV-cm}^2/\text{mg}$. So we get that: $b = 1 \text{ mA}$ \Rightarrow $Q_{\text{crit}}=0.2 \text{ PC}$ \Rightarrow LET=$20 \text{ MeV-cm}^2/\text{mg}$.

Connect the model to one of the sensitive node of the three new latches, get Table 4 (when the value of $b$ become the biggest current, the sensitive note will not recover, and the stored state will be wrong).

From Table 4, we can see the SEU-immunity of the NHIT latch is weaker than that of the NDICE latch, and then, we generally define it as crashing SEU-immunity when its LET$_{\text{th}}$ is above $100 \text{ MeV-cm}^2/\text{mg}$ according to the former experience. At last we know that the NDICE latch has
the best compositive capability and the best SEU immunity.

Table 4: The SEU-immunity of the three new latches.

<table>
<thead>
<tr>
<th>New latch</th>
<th>The biggest current (b)</th>
<th>LET</th>
</tr>
</thead>
<tbody>
<tr>
<td>NHIT latch</td>
<td>3.375 mA</td>
<td>67.5 MeV-cm²/mg</td>
</tr>
<tr>
<td>NDICE latch</td>
<td>&gt;5 mA</td>
<td>&gt;100 MeV-cm²/mg</td>
</tr>
<tr>
<td>NGDICE latch</td>
<td>&gt;5 mA</td>
<td>&gt;100 MeV-cm²/mg</td>
</tr>
</tbody>
</table>

REFERENCES