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Short Course SC001

From Tool Development to Modeling Realistic Product Structures

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Tuition Fee: (USD 200)

Course Objective:

Rapid advances in IC and packaging performance require increasingly more powerful electrical parameter extraction tools. The problem sizes commensurate with multi-GHz operation require millions-of-unknowns solutions for RLC and full-wave analyses. Both problem size and run times need to be improved by orders of magnitude. In this half day short course, we are investigating advanced techniques to solve such practical interconnect and packaging problems.

Who Should Attend:

The course is designed for chip/package designers and researchers who need to develop methodologies for 2D and 3D electromagnetic analysis of product level geometries.

Course Outline:

1. Fundamentals and examples for 2D capacitance and inductance-resistance extraction (per-unit-length).
2. Guidelines and common mistakes/misconceptions for per-unit-length extraction.
3. Guidelines for 3D full-wave problem setup and S-parameter solutions using advanced MoM field solver.
4. Identifying mesh quality issues in 3D full wave extraction.
5. Working understanding of domain decomposition and FFT based accelerated techniques.
6. Fundamental understanding of 3D capacitance extraction.
7. Accelerated hierarchical 3D capacitance extraction of on-chip and packaging interconnects.
8. Parallel 3D capacitance extraction.

PART I. GENERAL 2D PARASITIC PARAMETER EXTRACTION

This section provides a fundamental understanding of the issues in calculating the RLCG parameters for two dimensional transmission line structures. We start by considering the basic geometry of the canonical structure and describe how to mathematically set-up and solve the 2D capacitance and 2D inductance-resistance problems, focusing on the matrix formulation and boundary conditions. We investigate theoretical, geometrical, and practical considerations associated with the extraction of parameters, including fringing field and eddy current effects, edge-effect and skin-depth considerations, loose and tight coupling, near-end and far-end noise, and gridding to assure accuracy. We address common misconceptions and mistakes made in modeling and interpreting the results. Lastly, we cover the more advanced issues of causality, covering causes and remedies. Solutions for actual problems will be demonstrated. Throughout the session, questions from the class attendees will be welcomed.

PART II. FULL WAVE 3D S-PARAMETER EXTRACTION

This section provides an understanding of the fundamentals of full wave extraction of 3D geometries, such as fan-outs, via arrays, meandering lines, etc. We will start by understanding good meshing practices for such examples. Then we will look at where and how to define ports when analyzing simple and then complicated structures, and review the S parameters outputs for these examples. For the larger structures, a domain decomposition approach can be useful to accelerate the solution. How to use such an approach and how to properly define domains for the best results will be presented. Finally, we will

demonstrate how to identify examples where domain decomposition is likely not appropriate, and describe the use of an alternate accelerated pre-corrected FFT based solutions for these example.

PART III. HIERARCHICAL CAPACITANCE EXTRACTION

This section will first discuss the differences between the direct boundary element method and indirect boundary element method for practical parasitic capacitance extractions of on-chip interconnects. Based on these discussions, a general hierarchical approach to extract the capacitance matrix is derived. The block capacitance matrix is constructed locally from the direct boundary element method. The binary tree browsing through matching boundary conditions shrinks the problem to the final global capacitance matrix. A significant merit of this method is that it has similar simulation complexity for homogeneous and inhomogeneous media problems. Examples on how to use this method for real on-chip interconnects and packaging problems are introduced and discussed. To improve the simulation capability, a parallel scheme based on this hierarchical approach is introduced and its efficiency is verified through benchmarks.

Instructor(s) Biography:

Barry J Rubin, Ph.D., is a research staff member at IBM's T. J. Watson Research Center, N.Y. He formerly worked on the circuit design of CMOS and charge-coupled devices and then in electrical package analysis, doing pioneering work on the understanding and calculation of signal propagation and delta-I noise in single and multi-chip ceramic modules. Dr. Rubin later focused on electromagnetic techniques: He developed the first rigorous technique for calculating the propagation parameters for signal lines and other features situated in a mesh plane environment; he developed the approach for using two-dimensional rooftop functions to model volume polarization effects; he developed comprehensive techniques using physically-based gridding to automatically refine meshes for conductor proximity effects; and he co-invented a robust technique for handling inhomogeneous structures. More recently, he developed reduced-coupling and other advanced techniques for handling large problems. He has worked on nearly all aspects of the electrical analysis of packages and been personally involved in the analysis of many generations of IBM server products. Dr. Rubin's work appears in numerous conference and journal articles. He has mentored dozens of engineers and interns, and he holds an IBM Fifth Plateau Invention Achievement Award.

Jason Morsey received the B.S. (with honors) and M.S. degrees in electrical engineering from Clemson University, Clemson, SC, in 1998 and 2000 respectively, and his Ph.D. degree in electrical engineering from the University of Illinois in 2003. Since 2003 Dr. Morsey has been with the IBM T.J. Watson Research Center, Yorktown Heights, NY, where he is a Research Staff Member in the Interconnect and Packaging Analysis group. He is the current Electrical Interconnect and Packaging chair on the IBM Professional Interest Community, which supports and encourages external professional interactions. His research interests include computational electromagnetics and fast electromagnetic solvers, modeling of high-speed interconnects, packaging analysis, and signal integrity analysis.

LIJUN JIANG received the B.S. degree in electrical engineering from the Beijing University of Aeronautics and Astronautics in 1993, the M.S. degree from the Tsinghua University in 1996, and Ph.D from the University of Illinois at Urbana-Champaign in 2004.
From 1996 to 1999, he was an application engineer with the Hewlett-Packard Company. From 2004 to 2005, he was a Postdoc with the IBM T.J. Watson Research Center. Since 2006 he has been with the IBM T.J. Watson Research Center as a research staff member. His research interests focus on the signal integrity analysis, computational Electromagnetics, EMC, antenna analysis and design, and numerical methods.
Dr. Jiang received the IEEE MTT-S Graduate Fellowship Award in 2003 and Y.T. Lo Outstanding Research Award in 2004. He is a member of the IEEE and a member of Sigma Xi. He serves as the reviewer of IEEE Transactions on Antenna & Propagation, and IEEE Transactions on Advanced Packaging.

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